

VFAT2 - Digital Specification (Version 5)

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Version No.	Date	changes w.r.t. previous version
1	February 2005	-
2	April 2005	Embedded channel specific registers
3	May 2005	Channel registers in main I2C block Number of registers defined
4	May 2005	Data format defined Floorplan added
5	May 2005	Identifiers added to Data Format VFAT2 to GOL connection defined

Table 1: Document history

This document is intended to provide the digital specification for the VFAT2 ASIC design. It is intended as a working document that will be continuously updated throughout the project design.

Project Design Engineers
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Table 2: Project design engineers

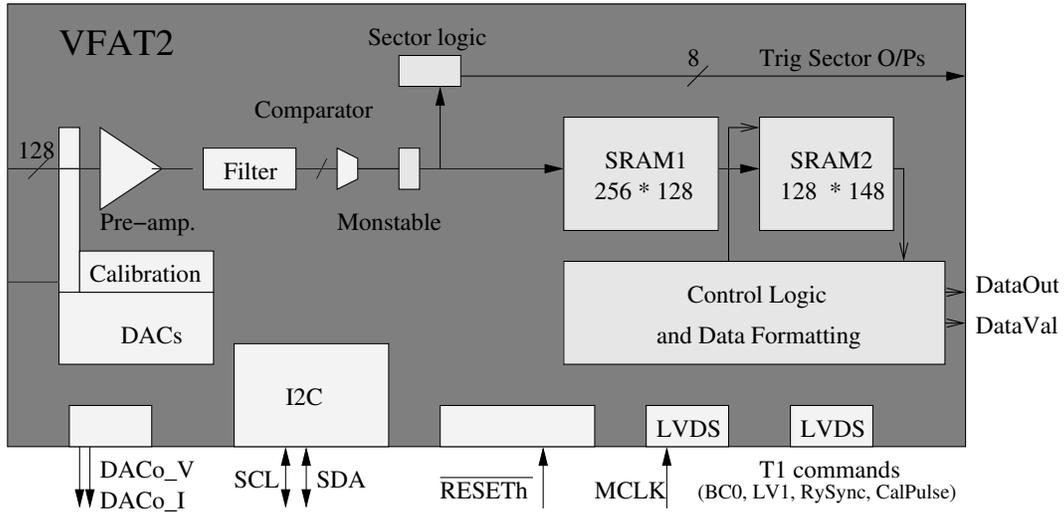


Figure 2: Block diagram of the VFAT2 chip.

programmable sectors which can be flagged with the fast OR in this way.

1.1 Triggering functions

Within TOTEM VFAT2 will provide fast regional hit information to be included within the CMS First Level Trigger.

Channels are grouped together to form sectors. A hit channel in a given sector will set an LVDS output assigned to that sector to a logic “1”.

The assignment of channels to sectors is programmable. There are 8 LVDS sector outputs labelled S1 to S8. Not all LVDS outputs need be used and the number sectors used can be selected between 1,2,4 and 8. Once the number of sectors have been chosen the channel assignment to the sector can be made with different options. The options are defined by the requirements of the physics needed from VFATs used with the Roman Pots and VFATs used with the GEM detectors. Further details of channel assignment to sectors is given in section 5.1.1.

1.2 Tracking functions

On receiving a LV1 signal, data corresponding to the triggered time slot is transferred to a second SRAM memory (SRAM2). The LV1 latency is not expected to exceed $6.4\mu\text{s}$ (256 clock periods). Hence, SRAM1 is dimensioned 256 by 128. SRAM2 contains only triggered data. It is dimensioned to be 128 by 148 for data plus headers, hence VFAT2 can store up to 128 triggered events of data for all channels at any one instant in time.

VFAT2 will label the data with 3 headers. These are the Bunch Crossing number (BCN 12 bits), Event number (EN 8 bits), and the chip Identification number (ID 16 bits). The BCN is generated by a 12 counter (BC) that increments every clock cycle and is reset to zero on receiving a BC0 T1 command via LVDS. The EN is generated by an 8 bit counter that increments for every LV1. It is also reset by a BC0 command or the *Clear* signal. Both counters are cyclic and return to zero at the end of the counter range.

As soon as SRAM2 has data the Read cycle begins. During the Read cycle a Data Formatting block streams out a binary data stream to the GOL. The chip operates with a continuous write/read operation without dead time.

1.3 T1 Commands

VFAT2 receives 2 LVDS signals namely the 40MHz master clock “MCLK” and a “T1” signal. The T1 signal is an encoded signal which contains 4 separate commands all synchronous with the MCLK. These 4 commands are decoded within the “Trigger Decoder” within the chip. The 4 command are: bunch crossing zero identifier (BC0), the level1 trigger “LV1”, a synchronous reset “ReSynch”¹ and a calibration timing pulse “Cal”.

The coding of the T1 commands is given in table 3.

Pattern	Command Name	Function
100	LV1A (Level 1 Accept)	Trigger
111	CalPulse	Timing of calibration pulse
110	ReSynch	Resynchronisation of all state machines
101	BC0	Bunch crossing zero identifier

Table 3: T1 Commands

2 Radiation Hardness and Single Event Upset (SEU) protection

The location of VFAT in the experiment means that the chips will be exposed to varying levels of ionising radiation, the design will therefore be made to withstand a

¹ReSynch : The ReSynch is a synchronous pulse, of 25ns period, that can be applied to VFAT2 to realign logical pointers in the control logic, FIFO and sequencer state machines. All counters need to be reset on a ReSynch. Register contents programmed through the I²C remain untouched. Application of a ReSynch signal will erase all data stored in VFAT2 awaiting readout. Depending on the state of VFAT2 at the moment of receiving a ReSynch, data corresponding from 0 to 64 LV1 triggers will be lost.

minimum total dose of 100 MRads(Si). For the digital circuitry a major concern is SEU through charge deposition from particles of high LET.

The logic blocks within VFAT2 essential for the control of the chip will have triplicated logic to protect against SEU.

2.1 Triplicated logic, testability through a “scan path” and counting upsets.

The I²C, programmable registers, control logic and the trigger sequencer will be protected from SEU by the use of triplicated flip-flops.

The production testing of these flip-flops will be achieved through a scan chain. C4I will provide details of how the scan chain works, I/Os needed and test vectors generated by synopsis. The scan chain should not rely on a 40MHz MCLK clock but have its own clock which is not used during the operation of the experiment.

In VFAT2, each set of triplicated flip-flops should also contain an output which goes high if there is a discrepancy between them ie. a 2 to 1 vote has taken place. A logic “OR” should be made of all of these outputs and the result used to increment an 8 bit synchronous counter. The result of the counter should be stored in an 8 bit register (UpsetReg) which is accessible via the I²C. The I²C can then be used to read back the contents of the register.

This is, in fact, a diagnostic tool for understanding the SEU environment in the experiment. It can also be used to detect a “stuck at” fault condition since the “OR” would always be high and the counter clocked to FF.

It is important that the counter counts from 0 to FF and stops at FF. It should be reset by the “*Clear*” signal.

3 The Operation Cycle

Figure 3 shows a flowchart of the operation cycle of VFAT2.

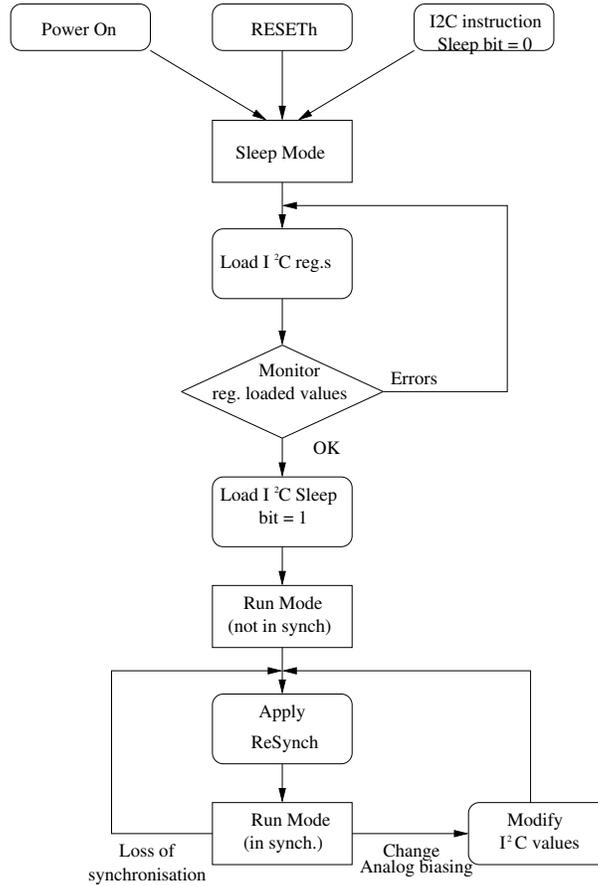


Figure 3: Flowchart of the operation cycle of VFAT2

A key point to the flowchart is direct entry into a “sleep” mode on applying power to the circuit. A power-on reset circuit generates a pulse that sets the internal programmable registers to default conditions. These default conditions mean that the chip is in a non-functional, minimum power consuming condition with only the I²C circuits remaining responsive.

Figure 4 shows a schematic representation of the circuit configuration. On PowerOn or on the application of a hard reset (\overline{RESETh}), an I²C reset is performed. At the same time multiplexers that switch between the register outputs and the internal functions are set to the default setting. The default setting is hard wired inside the chip.

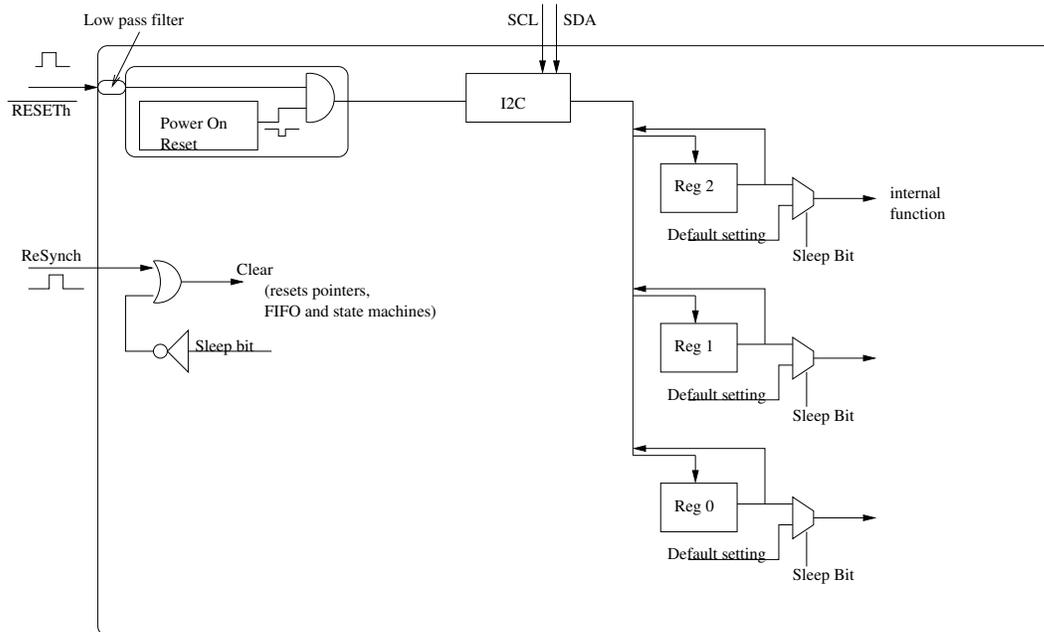


Figure 4: A schematic view of the programmable registers.

4 The I²C interface

4.1 I²C SEU Protection

The function of the I²C will be protected against single event upset. Both the main I²C block and the programmable registers should be protected against SEU through triplicated logic.

4.2 I²C requirements

A summary of the main requirements of the I²C port is given in table 4

1,	Should work correctly with all functions of the CCU
2,	Should be compatible with standard I ² C “off the shelf” chips for test purposes
3,	Should be triplicated to guard against SEU
4,	The application of a (\overline{RESETh}) will reset the I ² C and apply sleep values to the registers .
5,	The chip address (7 bit) will be assigned by connections external to the chip. Hence the 8 bit I ² C address bus should be available to take to pads.
6,	The input pads for the SDA and SDL lines should have hysteresis and rail to rail glitch protection.

Table 4: I2C specifications

5 Programmable registers

There are a number of programmable features in VFAT2 accessible through the I²C port on each chip. There will be a control registers, data registers and a chip ID.

5.1 The Control Registers

VFAT2 will have two “Control Registers” labelled Control register 0 and Control register 1 which will have bit allocation as shown in tables 5 and 6 .

7	6	5	4	3	2	1	0
	FEpolarity	CalMode ⟨1⟩	CalMode ⟨0⟩	Trigmode ⟨2⟩	TrigMode ⟨1⟩	TrigMode ⟨0⟩	Sleep/Run Sleep/Run

Table 5: Control Register 0

7	6	5	4	3	2	1	0
-	-	-	ProbeMode	DACsel	DACsel	DACsel	DACsel
-	-	-	-	⟨3⟩	⟨2⟩	⟨1⟩	⟨0⟩

Table 6: Control Register 1

The function of the bits are as shown in table 7.

Bit name	Function
Sleep/Run	0 = Sleep (Default), 1 = Run
TrigMode⟨1 : 0⟩	Trigger mode settings : as in table 8
CalMode⟨1 : 0⟩	Calibration settings : as in table 10
CalPrec	Selects calibration precision, 0 = low (LP)(default) and 1 = high (HP)
FEpolarity	Front-end polarity - defines the signal polarity from the sensor 0 = positive I/P signal (default), 1 = negative I/P signal (also sets the CalPulse to a positive or negative pulse)
DACsel⟨3 : 0⟩	Controls DAC selection for DCU monitoring, see table 9

Table 7: Bit function of the control registers

5.1.1 Trigger Sector Configurations

The selection of the trigger functions through the TrigMode bits are detailed in table 8.

TrigMode $\langle 2 \rangle$	TrigMode $\langle 1 \rangle$	TrigMode $\langle 0 \rangle$	Function
0	0	0	No Trigger (default)
0	0	1	One sector (S1)
0	1	0	Four sectors (S1 to S4)
0	1	1	Eight sectors (S1 to S8)
1	X	X	GEM mode (Sectors to be defined)

Table 8: TrigMode functions.

VFAT2 has a number of possible trigger modes (TrigMode) defined by the combination of 3 bits (TrigMode $\langle 2 : 0 \rangle$) shown in table 8. The trigger functions are different depending on whether VFAT2 is used with the Roman Pots or with the GEM detectors. Bit TrigMode $\langle 2 \rangle$ is used to tell VFAT2 if it is in Roman Pot mode or GEM mode.

In Roman Pot mode Trig $\langle 2 \rangle$ is 0 and bits TrigMode $\langle 1 : 0 \rangle$ are used to define 4 sector configurations. There are 8 possible sector outputs within VFAT2. If all 8 are chosen by setting the TrigMode to 011 then the 128 channels are divided into eight equal regions. Sector 1 (S1) will contain channels 1 to 16, sector 2 (S2) will contain channels 17 to 32 etc. If 4 sectors are chosen by setting the TrigMode to 010 then the 128 channels are divided into four equal regions. Sector 1 (S1) will contain channels 1 to 32, sector 2 (S2) will contain channels 33 to 64 etc. The unused LVDS output drivers will be shut down to conserve power.

In GEM mode, bit TrigMode $\langle 2 \rangle$ is 1 and bits TrigMode $\langle 1 : 0 \rangle$ are used to define GEM sector configurations. These GEM sector configurations are complex combinations of channels and at the time of writing have yet to be defined.

5.1.2 Measuring internal DAC response

Each DAC response is to be measured periodically in order to apply the correct settings for biasing. VFAT2 will have two outputs labelled “DACo-I” and “DACo-V”. These outputs will be fed to the DCU chip which has an on board ADC and the measured value read back in digital form through the DCU chip I²C.

A switching mechanism is therefore required in VFAT2 to route (one by one) the output of each current DAC to DACo-I, and each voltage DAC to DACo-V. The selection of the DACs is controlled by bits DACsel $\langle 3 : 0 \rangle$, see table 9.

DACsel<3>	DACsel<2>	DACsel<1>	DACsel<0>	Function
0	0	0	0	Normal Running (default) (DACo-V “low”, DACo-I “Hi Z”)
0	0	0	1	IPreampIn to DACo-I (DACo-V “low”)
0	0	1	0	IPreampFeed to DACo-I (DACo-V “low”)
0	0	1	1	IPreampOut to DACo-I (DACo-V “low”)
0	1	0	0	IShaper to DACo-I (DACo-V “low”)
0	1	0	1	IShaperFeed to DACo-I (DACo-V “low”)
0	1	1	0	IComp to DACo-I (DACo-V “low”)
0	1	1	1	IThreshold1 to DACo-I (DACo-V “low”)
1	0	0	0	IThreshold2 to DACo-I (DACo-V “low”)
1	0	0	1	VCal to DACo-V (DACo-I “hiZ”)
1	0	1	1	CalOut to DACo-V (DACo-I “hiZ”)
1	1	*	*	Spare

Table 9: VFAT2 DACs to DCU control

5.1.3 Calibration functions

VFAT2 includes an internal calibration circuit. This circuit delivers an electronic test pulse to an injection capacitor at the input of a given channel (see section 5.5 for channel selection) therefore applying a charge pulse to the preamplifier. The amplitude of the electronic test pulse is governed by a DAC (VCAL) and is programmable.

However, before applying a calibration pulse the calibration circuit response must be calibrated. For this one must connect the calibration circuit output (CalOut) to the DCU as shown in table 9 with setting 0110 (VCal to DACo-V). Measuring the amplitude of the voltage step is done in two stages. The first step is to measure the baseline of the voltage step to be injected ($\text{CalMode}\langle 1 : 0 \rangle = 01$). The second step is to measure the peak of the amplitude for each DAC setting ($\text{CalMode}\langle 1 : 0 \rangle = 10$ while scanning all values of the VCAL DAC). The difference between the two is the voltage step applied for each VCAL DAC setting.

It is also possible to apply an external voltage pulse to a given channel by setting $\text{CalMode}\langle 1 : 0 \rangle = 11$ for test purposes in the lab. This latter mode will not be used during the running of the experiment.

The selection of calibration functions through the CalMode bits are detailed in table 10.

5.2 The Chip ID registers

There will be a 24 bit chip ID contained within three Chip-ID registers called ChipID3 (ID23(MSB) - ID16), ChipID2 (ID15(MSB) - ID8) and ChipID1 (ID7 -

CalMode<1>	CalMode<0>	Function
0	0	Normal running (default)
0	1	CalOut = Baseline (possible to connect to DACo-V)
1	0	CalOut = VCal (possible to connect to DACo-V)
1	1	CalOut = External calibration pulse (not possible to connect to DACo-V)

Table 10: CalMode functions.

ID0(LSB)). The 24 bits will be defined by a set of fuses which will be laser blown on wafer. The I²C interface and register block will therefore be presented with a 24 bit ID.

5.3 The latency register (LAT)

There will be one 8 bit register for programming the LV1 latency into the chip. Each bit represents one clock cycle of latency. The latency can be programmed from 1 to 256 clock periods (ie. up to 6.4 μ s). The default setting is 1000 0000 (=128 clock cycles).

5.3.1 The Upset register (UpsetReg)

The result of the Upset counter (explained in section 2.1) is stored in the Upset register bit for bit as in table 11.

7	6	5	4	3	2	1	0
UpsetCounter<7> (MSB)	<6>	<5>	<4>	<3>	<2>	<1>	UpsetCounter<0> (LSB)

Table 11: The Upset register (UpsetReg)

5.4 The Channel Registers (ChanReg)

There are 128 channels in VFAT2. Whilst most programmable settings are common to all channels there are some settings which need to be channel specific. These include the “CalChan” command, “MASK” and “TrimDAC” setting. To accomodate these channel specific commands each channel will be assigned an 8 bit ChanReg. There will hence be 128 Channel registers labelled ChanReg<1 : 128 > for channels 1 to 128.

7	6	5	4	3	2	1	0
-	CalChan	Mask	TrimDAC <4>	TrimDAC <3>	TrimDAC <2>	TrimDAC <1>	TrimDAC <0>

Table 12: The Channel Specific register (ChanReg)

The register will be embedded in the analog channel together with the register address. This avoids multiple metal lines crossing the channels. However, there will still be some I2C signals crossing all channels. It is hence important that the I2C is powered from the analog power supply.

5.5 The calibration channel selection

The internal calibration pulse can be delivered to any individual channel and any number of channels simultaneously. To do this bit “6” of each channel’s ChanReg is devoted to this function. The default setting for each bit is 0 which is for normal running. A logic 1 is for applying the calibration pulse to the specified channel.

5.6 Masking a channel

Each channel has to have the possibility of being masked in order to silence a noisy channel. This requires 1 Mask bit per channel. Bit “5” of the ChanReg is used for this function. The default setting for each bit is 0 which is for normal running (an active channel). A logic 1 is for applying the Mask, effectively switching off that particular channel.

5.7 Fine adjustment of the comparator threshold

The course setting for the threshold of the comparators will be made via a DAC labelled ThReg. This is common for all channels. The VFAT sensor has varying levels of input capacitance which can have a small effect on the gain of a given channel. The gain may also be modified by exposure to very high levels of radiation. Some channels

may receive more radiation than others resulting in varying levels of gain. Hence fine adjustment of the threshold on a channel by channel basis could be necessary. To prepare for this each channel will be equipped with a 5 bit Trim DAC. Bits ChanReg(4 : 0) are allocated for this function.

5.8 The DAC registers

There will be a number of DACs controlling the analog variables. These are IPreampIn, IPreampFeed, IPreampOut, IShaper, IShaperFeed, IComp, IThreshold1, IThreshold2 and VCal. Each of these DACs has an 8 bit register associated with it which can be set via the I²C.

5.8.1 Sleep Settings

The sleep settings for the defined registers are given in tables 13.

Reg. Name	Sleep setting	Sleep value	Reg. Add.	Reg type
Cont.Reg⟨0⟩	0000 0000		0	W/R
Cont.Reg⟨1⟩	0000 0000		1	W/R
VCal	1000 0000	$\sim 1V$	2	W/R
IPreampIn	0000 0001	$\sim 1\mu A$	3	W/R
IPreampFeed	0000 0001	$\sim 1\mu A$	4	W/R
IPreampOut	0000 0001	$\sim 1\mu A$	5	W/R
IShaper	0000 0001	$\sim 1\mu A$	6	W/R
IShaperFeed	0000 0001	$\sim 1\mu A$	7	W/R
IComp	0000 0001	$\sim 1\mu A$	8	W/R
ChipID⟨0⟩			9	RO
ChipID⟨1⟩			10	RO
ChipID⟨2⟩			11	RO
UpsetReg.	0000 0000		12	RO
PointerReg	0000 0000		13	W/R
PointerData	0000 0000		14	W/R
Lat	1000 0000		*0	W/R
ChanReg⟨1 : 128⟩	0000 0000		*1 to *128	W/R
IThreshold1	0000 0001	$\sim 1\mu A$	*129	W/R
IThreshold2	0000 0001	$\sim 1\mu A$	*130	W/R
CalPhase	0000 0000		*131	W/R
Spare⟨1 : 4⟩	0000 0000		*132 to *135	W/R
* → addressed via registers 13 and 14				

Table 13: The VFAT2 Register Sleep settings

6 The Masked Monostable Block

This block basically consists of a clocked monostable.

Figure 5 shows a block diagram for the channel from the shaper output through to SRAM1.

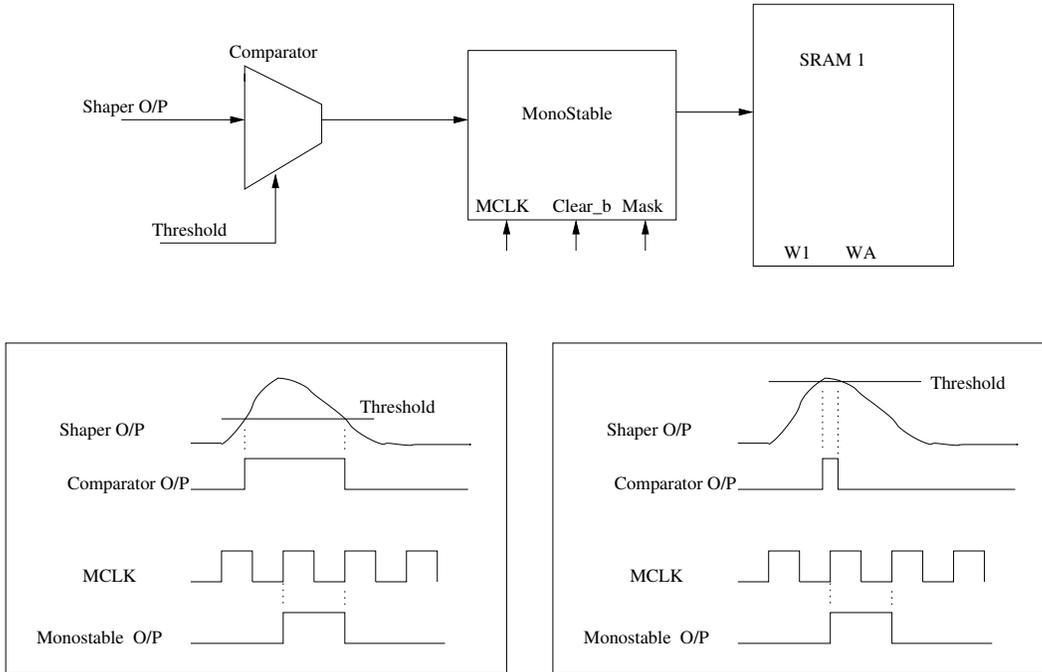


Figure 5: Block diagram of the masked monostable block.

The comparator is at present an asynchronous comparator without hysteresis. On passing a programmable threshold the comparator output goes high and returns low again when decending back through the threshold. For very large signals the comparator output may remain high for more than one clock cycle. Also if the signal barely passes threshold the comparator output may go high for less than one clock period. Both cases should trigger the monostable which should provide a pulse of one clock period only. It is this pulse which is sampled by SRAM1.

The mask bit can be used to disable the channel and force the monostable output to be always zero as in table 14.

Mask bit	Function
0	Normal operation (default)
1	Masked (Monostable output = 0)

Table 14: Mask bit functions.

7 Logic Blocks

7.1 Control Logic

The Control Logic contains a “Write State Machine” and counters for the BCO, EN and Upset counter. Figure 6 shows in a block diagram format these building blocks. All of these state machines are clocked by the 40MHz master clock and transitions take place on the rising edge.

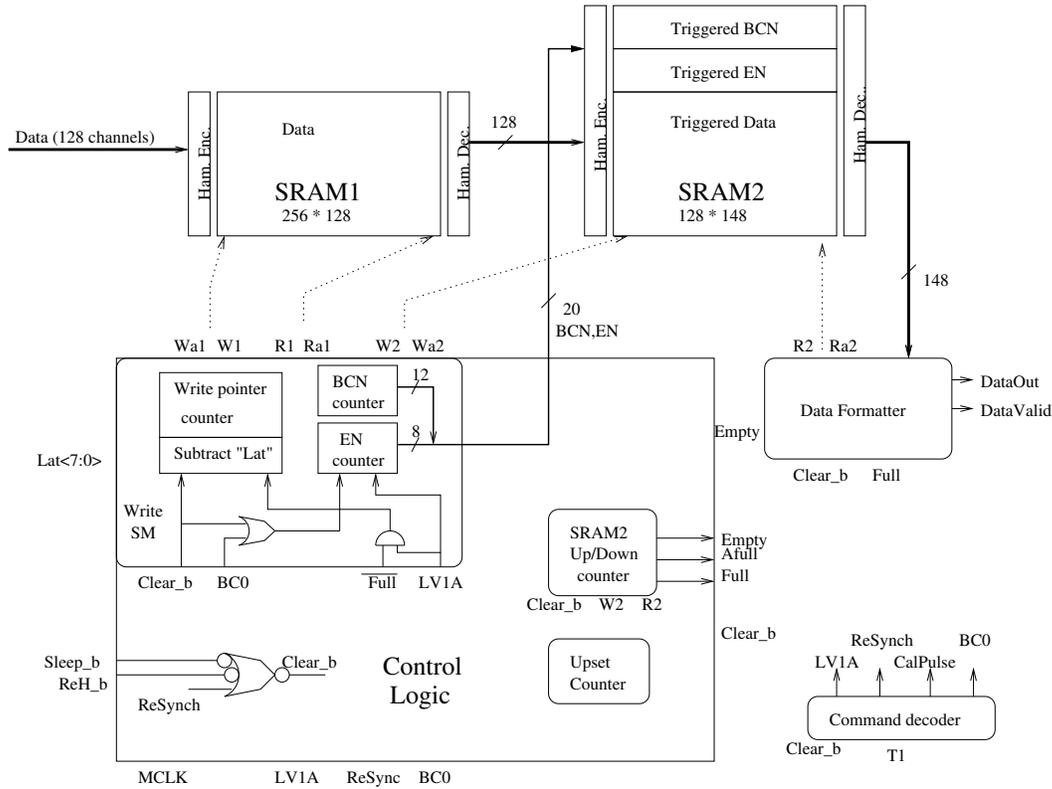


Figure 6: The Control Logic.

VFAT2 contains two SRAM blocks. Each 25ns the comparator outputs are sampled and the results stored in parallel in the first of the SRAM blocks (SRAM1). On receiving a trigger (LV1) the data stored in SRAM1 corresponding to the time slot that initiated the LV1 is transferred to the second SRAM (SRAM2). SRAM2 will therefore contain “hit” information for each channel for triggered events.

7.1.1 The Write State Machine

The “Write SM” controls the timing of the signals used for sampling the outputs of the comparators at 40MHz and for transferring triggered data from SRAM1 to SRAM2. Wa is the write address, W is the write signal, Ra is the read address and R is the read signal.

It contains the Write Pointer, Bunch Crossing Number (BCN) and Event Number (EN) counters.

The Write Pointer counter is a cyclic 8 bit counter that increments every clock period providing the write address “Wa”. It is reset to zero on receiving a Clear signal.

The BCN counter is a cyclic 12 bit counter that increments for every clock period. It is reset to zero on receiving a Clear signal.

The EN counter is a cyclic 8 bit counter that increments for every LV1A. It is also reset to zero on receiving a Clear signal.

The function of the Write State machine is as follows: The “write pointer counter” provides “Wa” for SRAM1 incrementing every clock period. On receiving an LV1A the channel data corresponding to the trigger is located by subtracting the Latency (Lat $\langle 7 : 0 \rangle$) number from the “Wa”, hence $Ra1 = Wa1 - Lat$. The triggered channel data is then transferred to SRAM2 together with the value of the BCN and EN counter.

Inputs	Outputs
<u>Clear</u> , MCLK, LV1A, Lat $\langle 7 : 0 \rangle$	Wa, W1, Ra1, R1, Wa2, W2, BCN $\langle 11 : 0 \rangle$, EN $\langle 7 : 0 \rangle$

Table 15: Write state machine I/Os

A timing diagram for the Write SM signal is shown in 7.

7.1.2 The Clear Signal

A signal “Clear” is defined as “RESETh” OR “ReSynch” OR “Sleep”. On release of the “Clear” signal the Write state machine starts.

7.1.3 SRAM2 up/down Counter

The generation of flags will be achieved via a 6 bit counter emulating the state of SRAM2. The counter should count up in steps of 1 for every W2 signal received. It should count down in steps of 1 for every R2 signal.

A number of flags need to be generated to satisfy internal VFAT, and possible system emulation functions. These are specified in table 16 along with the thresholds for each.

LV1s will also be blocked if they are received within the latency period following a ReSynch signal. Logically, an LV1 received during this period would relate to an event before or during the ReSynch and is hence not valid and is rejected.

Write State Machine timing diagram

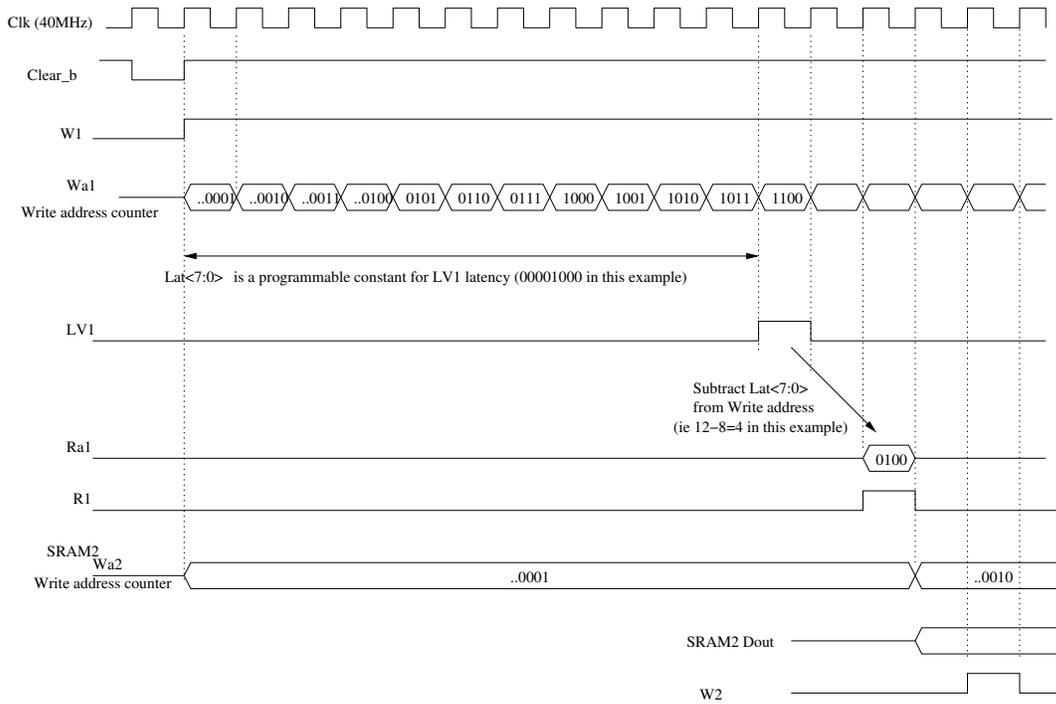


Figure 7: Timing diagram for the Write State Machine.

Flag	Flag generator counter =	Corresponding no. of stored LV1s	Action within VFAT
EMPTY	0	0	Start the “read” state machine on the “Empty” to “Not empty” transition
AFULL	126	127	No action inside VFAT Possible system emulator LV1 throttle
FULL	127	128	Inhibit further reception of LV1s by VFAT when this flag is set. The SRAM2 will fill to a maximum depth of 64.

Table 16: Flags used in the VFAT2.

7.2 The Data Formatter

The data format is defined as in figure 8.

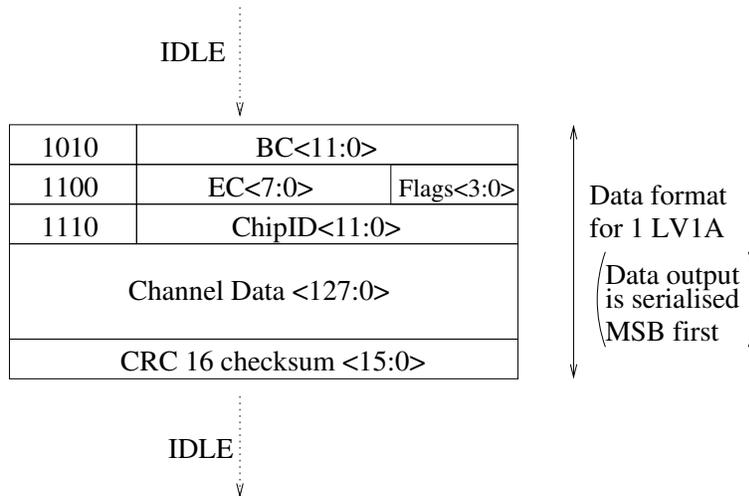


Figure 8: FAT2 data field format

The data exits the VFAT chip serially through an LVDS output pad called “DataOut”. The data field will exit the chip for each LV1A in the form given in figure 8 MSB first. Hence the first bit is the MSB of the BC number and the last bit is the LSB of the checksum.

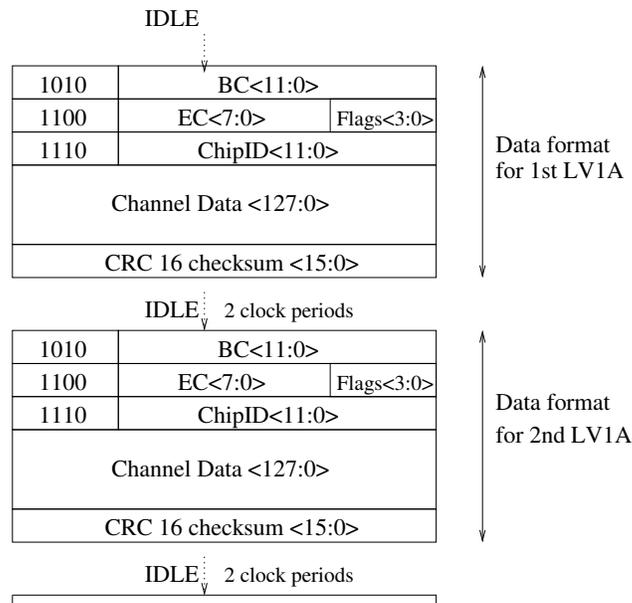


Figure 9: The data format for multiple triggers

If more than one LV1A has been stored in VFAT2 then data fields (corresponding to each LV1A) will exit the chip one after the other following a FIFO order. Each

data field is separated by two clock periods which are called “IDLE”. This is shown in figure 9. Hence the total time for the readout of 1 LV1A is 192 clocks for the data field plus 2 clocks for the IDLE period, this gives a total of 194 clock periods (4.85 μ s).

Another LVDS output “DataValid” goes high for the duration of the datafield and returns low to signify an IDLE period. Figure 10 shows the timing of this signal.

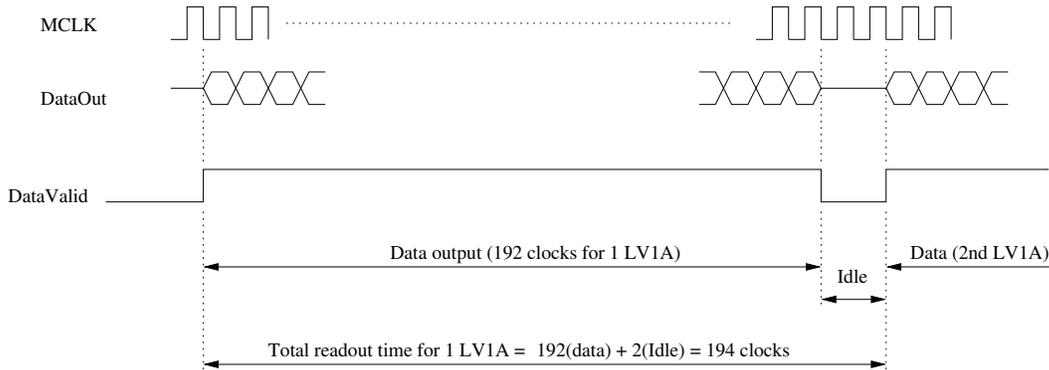


Figure 10: The DataValid signal

For TOTEM, it is foreseen to connect upto 16 VFAT2s to one GOL. Figure 11 shows this in block diagram format. The DataValid signal is connected from one VFAT2 to the “DAV/tx en” pin of the GOL (the CAV/tx er pin of the GOL should be tied low).

All VFAT2s will be synchronous and output their data at the same time. Hence following an LV1A, the “DataValid” signal goes high and the first bit of the data field for each VFAT2 is sent to each VFAT2s DataOut pin. The GOL will multiplex these bits within one clock cycle creating a 800M Bit/s stream. The bit data at the output of VFAT2 changes every 25ns. When the datafield has finished, the “DataValid” signal returns low commanding the GOL to generate IDLE patterns.

The state machine that controls the output of data should be clocked on the negative edge of the MCLK. This is so that the data is 180 degrees out of phase with the master clock making it easier to avoid timing errors by the GOL.

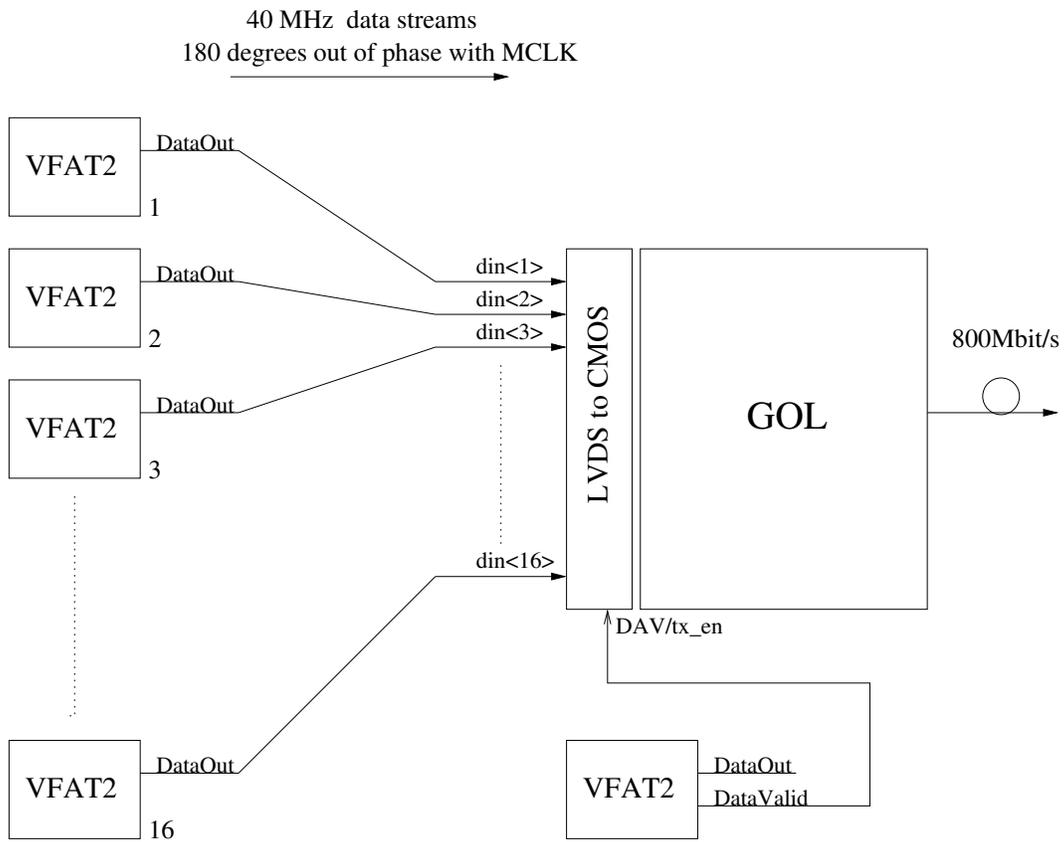


Figure 11: Connection between VFAT2 and GOL

7.3 Scan Chain

The Scan chain enables the testing of all flip flops in the Control Logic to detect fabrication errors. When put into “ScanMode”, all flip flops are cascaded. A serial pattern can then be clocked into “ScanIn”. This serial pattern will pass through all flip flops and exit the chip through “ScanOut”. If all flip flops are operational then the two patterns will match.

This test is useful because a faulty flip flop may not be noticed at the operation level because of the voting mechanism. Hence it would go unnoticed if only functional testing was employed. The Scan Chain however will find a flip flop with a “stuck at 1 or 0” condition.

If a number of VFAT2s are mounted on a board then the Scan chain inputs and outputs can be daisy chained together as in figure 12. All chips may then be tested at the same time.

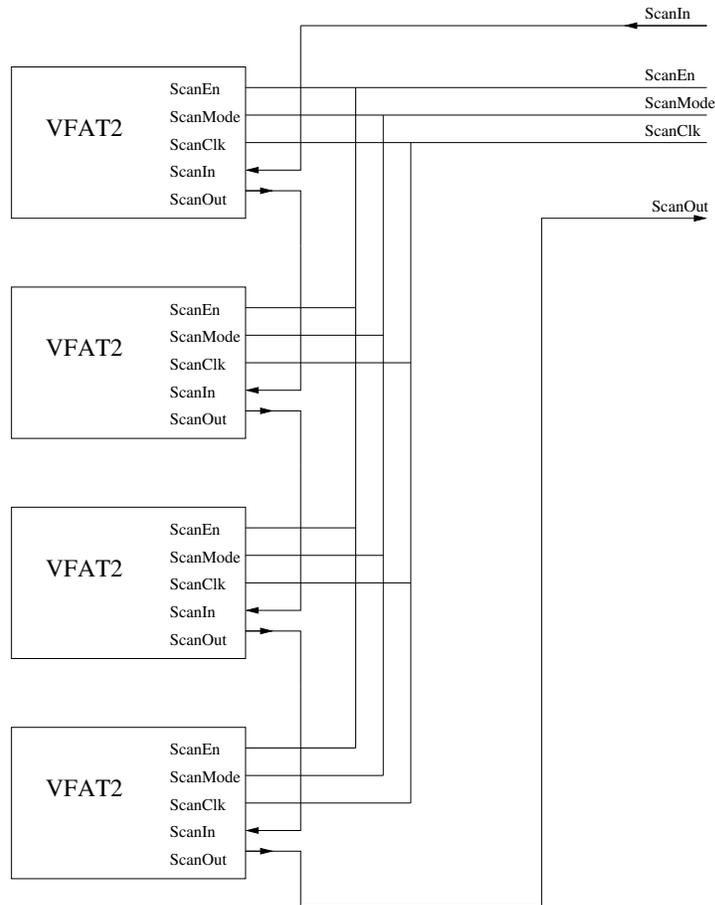


Figure 12: Daisy chaining of chips for Scan Chain testing.

8 Pad list

The floorplan for VFAT2 is given in figure 13

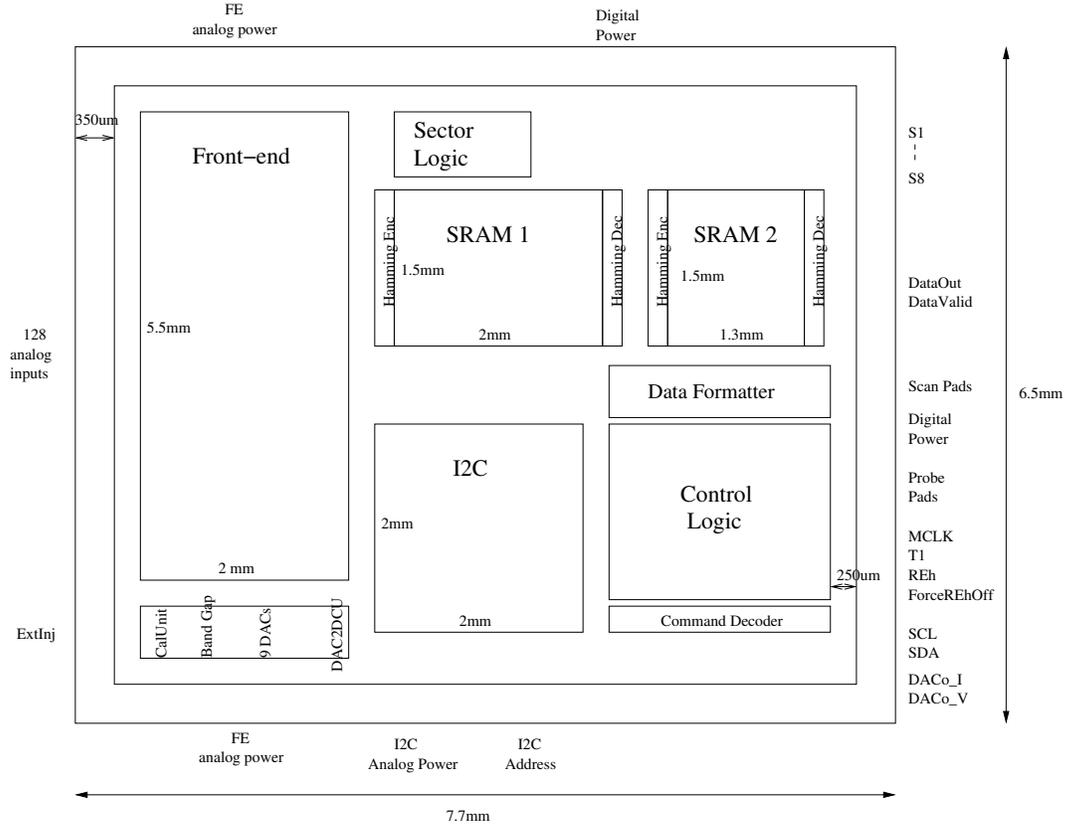


Figure 13: VFAT2 floorplan

A pad list corresponding pad list is given in tables 17, 18, 19 and 20 for the 4 sides of the chip.

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
1-128	In< 0 : 127 >	A,I	Analog input from sensor	?	?	Ext
129	ExtInj	A,I	test input	?	?	No

Table 17: VFAT2 pad list (left hand side, from top to bottom)

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
130	gnd!	power	FE pad ring	?	?	Ext.
131	vdd!	power	FE pad ring	?	?	Ext.
132	gnd!	power	FE guard ring	?	?	Ext.
133	vdd!	power	FE guard ring	?	?	Ext.
134	gnd!	power	FE return	?	?	Ext.
135	gnd!	power	FE return	?	?	Ext.
136	gnd!	power	FE return	?	?	Ext.
137	vdd!	power	FE vdda	?	?	Ext.
138	vdd!	power	FE vdda	?	?	Ext.
139	vdd!	power	FE vdda	?	?	Ext.
140	gnd!	power	I2C guard ring	?	?	Ext.
141	vdd!	power	I2C guard ring	?	?	Ext.
142	gnd!	power	I2C return	?	?	Ext.
143	vdd!	power	I2C vdda	?	?	Ext.
144-150	ChipAdd< 0 : 6 >	D,I	Chip address	?	?	Ext.
151	gnd!	power	I2C pad ring	?	?	Ext.
152	vdd!	power	I2C pad ring	?	?	Ext.

Table 18: VFAT2 pad list (bottom side, from left to right)

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
153	DACo-V	A,O	Voltage output	?	?	Ext.
154	DACo-I	A,O	Current output	?	?	Ext.
155	SDA	D,I/O	I2C	?	?	Ext.
156	SCL	D,I	I2C	?	?	Ext.
157	ForceREhOff	D,I	bond to gnd	?	?	Int.
158	REh-B	D,I	Hard Reset	?	?	Ext.
159-160	T1(B)	D,I	LVDS pair	?	?	Ext.
161-162	MCLK(B)	D,I	LVDS clock (40MHz)	?	?	Ext.
163	pb LV1A	D,O	Logic test pin	?	?	No
164	pb CalPulse	D,O	Logic test pin	?	?	No
165	pb ReSync	D,O	Logic test pin	?	?	No
166	pb BC0	D,O	Logic test pin	?	?	No
167	pb ??	D,O	Logic test pin	?	?	No
168	pb ??	D,O	Logic test pin	?	?	No
169	pb ??	D,O	Logic test pin	?	?	No
170	pb ??	D,O	Logic test pin	?	?	No
171	pb EMPTY	D,O	Logic test pin	?	?	No
172	pb AFULL	D,O	Logic test pin	?	?	No
173	pb FULL	D,O	Logic test pin	?	?	No
174	pb W1	D,O	Logic test pin	?	?	No
175	pb R1	D,O	Logic test pin	?	?	No
176	pb W2	D,O	Logic test pin	?	?	No
177	pb R2	D,O	Logic test pin	?	?	No
178	ScanOut	D,O	Scan chain	?	?	test
179	ScanIn	D,I	Scan chain	?	?	test
180	ScanClk	D,I	Scan chain	?	?	test
181	ScanMode	D,I	Scan chain	?	?	test
182	ScanEn	D,I	Scan chain	?	?	test
183	gnd!	power	digital guard ring	?	?	Ext.
184	vdd!	power	digital guard ring	?	?	Ext.
185	vdd!	power	digital (vddd)	?	?	Ext.
186	vdd!	power	digital (vddd)	?	?	Ext.
187	vdd!	power	digital (vddd)	?	?	Ext.
188	gnd!	power	digital return	?	?	Ext.
189	gnd!	power	digital return	?	?	Ext.
190	gnd!	power	digital return	?	?	Ext.
191-192	DataValid	D,O	LVDS pair	?	?	Ext.
193-194	DataOut	D,O	LVDS pair	?	?	Ext.
195-196	S8	D,O	LVDS pair	?	?	Ext.
197-198	S7	D,O	LVDS pair	?	?	Ext.
199-200	S6	D,O	LVDS pair	?	?	Ext.
201-202	S5	D,O	LVDS pair	?	?	Ext.
203-204	S4	D,O	LVDS pair	?	?	Ext.
205-206	S3	D,O	LVDS pair	?	?	Ext.
207-208	S2	D,O	LVDS pair	?	?	Ext.
209-210	S1	D,O	LVDS pair	?	?	Ext.

Table 19: VFAT2 padlist (right hand ²⁵side, upwards from the bottom)

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
211	gnd!	power	LVDSdrivers guard ring	?	?	Ext.
212	vdd!	power	LVDSdrivers guard ring	?	?	Ext.
213	vdd!	power	LVDSdrivers vddd	?	?	Ext.
214	vdd!	power	LVDSdrivers vddd	?	?	Ext.
215	vdd!	power	LVDSdrivers vddd	?	?	Ext.
216	gnd!	power	LVDSdrivers return	?	?	Ext.
217	gnd!	power	LVDSdrivers return	?	?	Ext.
218	gnd!	power	LVDSdrivers return	?	?	Ext.
219	vdd!	power	digital (vddd)	?	?	Ext.
220	vdd!	power	digital (vddd)	?	?	Ext.
221	vdd!	power	digital (vddd)	?	?	Ext.
222	gnd!	power	digital return	?	?	Ext.
223	gnd!	power	digital return	?	?	Ext.
224	gnd!	power	digital return	?	?	Ext.
225	vdd!	power	FE vdda	?	?	Ext.
226	vdd!	power	FE vdda	?	?	Ext.
227	vdd!	power	FE vdda	?	?	Ext.
228	gnd!	power	FE return	?	?	Ext.
229	gnd!	power	FE return	?	?	Ext.
230	gnd!	power	FE return	?	?	Ext.

Table 20: VFAT2 padlist (top side, from right to left)

The active signals that are transmitted to and from VFAT2 are shown in table 21. Global signals are shared between more than one chip while “Unique” signals are specific to an individual chip.

Signal No.	Signal Name	An./Dig., I/O	function	Unique or Global
1	REh-B	D,I	Hard Reset	Global
2-3	MCLK(B)	D,I	LVDS clock (40MHz)	Global
4-5	T1	D,I	LVDS pair	Global
6	SCL	D,I	I2C	Global
7	SDA	D,I/O	I2C	Global
8-9	DataOut	D,O	LVDS pair	Unique
10-11	S1	D,O	LVDS pair	Unique
12-13	S2	D,O	LVDS pair	Unique
14-15	S3	D,O	LVDS pair	Unique
16-17	S4	D,O	LVDS pair	Unique

Table 21: The signal list transmitted to and from VFAT2

Hence the number of active signals feeding a hybrid ($N_{HybridSignals}$) is the number of unique VFAT2 signals (N_{unique}) multiplied by the number of VFATs on a hybrid (N_{VFATs}) plus the number of Global signals (N_{Global}) as in equation 1. With 4 VFATs on a hybrid the number of asctive signals in a cable is 55. The number of power lines is in addition to this and should be maximised.

$$N_{HybridSignals} = (N_{unique} \cdot N_{VFATs}) + N_{Global} \quad (1)$$

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