## LCT-COMP ASIC chip

#### 1- Description

The LCT-COMP is a full ASIC integrated circuit designed in a  $0.7\mu m$  nwell technology from Alcatel-Mietec in Belgium.

It is a 16-Channels circuit with 1 extra channels on each side to insure the readout continuity from chip to chip; fig. 1 shows the general schematic of the circuit and fig. 4 shows the layout. Each channels is made of a 3.5 gain AC amplifier followed by a bench of three comparators and a piece of logic (TRIAD logic) which code on the output the status of the charge level on this channel compare to the left and the right channels.

#### 1-1 <u>AC amplifier</u>

The AC amplifier has a pulse gain of 3.5 and a DC gain of 0. It is made of an Operational Transconductance Amplifier with a capacitive element [Fig.: 2] in the feedback and also an OTA to stabilise the output offset compare to a reference level. The input can accept dc variations of  $\pm$  100mv without measurable change at the output and the output rise time is 50ns.

#### 1-2 Array of comparators

There are 3 comparators per channel (1 to 16), but only one in the channels 0 and 17, their output can be connected respectively to the previous chip and to the next chip to insure the readout continuity.

Three channels [Fig. 3] are always involved in the comparison process: channel Qn is compare to a threshold and compare to channel Qn+1 while channel Qn-1 is compare to channel Qn+1. The threshold is common to the 16 channels and adjustable through an outside pin; the offset of the other comparators can be adjusted as well to avoid oscillations.

#### 1-3 TRIAD logic

The 48 outputs of the comparators are feed in a logic circuit which group 2 channels in one output in order to minimise the number of connections to the next part of the circuit; a 40MHz clock sequence the outputs. Each output give on a 3-bits code the charge status at the inputs; if channel N and N+1 are concerned, 100 is a hit on N with the maximum of charge on  $\{N-1 \le N\}$ , 101 is a hit on N with  $\{N \ge N+1\}$ , 110 is a hit on N+1 with  $\{N \le N+1\}$  and finally 111 is a hit on N+1 with  $\{N+1 \ge N+2\}$ .

The time of action of the logic can be adjusted around the peaking time of the input signals by a 3-bits code.

### 2- Pre-production: results of tests.

Some characteristics of the LCT-COMP can fluctuate from channel to channel or from chip to chip, the AC gain and the output DC level of the input amplifier, the offsets of the comparators and the thresholds. These fluctuations are only measurable through the offsets and thresholds.

The prototype fabrication having given good results, a fabrication of 2 wafers (540 chips) has been decided and 150 chips have been tested.

The yield is 66%; the loss is mainly given by functionality fault, and some chips have been rejected because of a too large fluctuation in the offsets or the thresholds.

The following histograms show respectively the gross spread of the thresholds, the maxmin difference of the thresholds and the spread of the L>R offset; the R>L offsets spread being negligible.

The testing should have been done on the IMS tester at CERN, but the socket of the testboard didn't fit exactly the pins of the package and gave some bad contacts. This Yamaichi socket has been sold for this package.

New sockets have been ordered, also guaranty for this package, and the automatic testing will start again after their mounting.







## **3-Production**

The full production of wafers can start before the end of 2000, followed by the plastic encapsulation. A specialised firm will do the testing of the chips. The tests procedure will take advantage of the automatic testing prepared at CERN.



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# LCT-COMP LAYOUT

