Configuration (CR) and control/status (CSR) in VME64, VME64x, VME64xP

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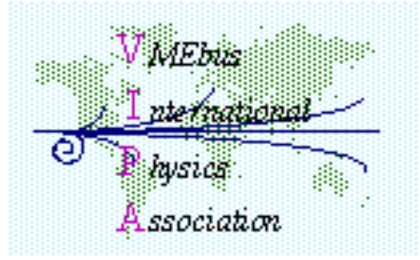
CERN

VME64 introduces CR/CSR space



- Defines optional A24 CR/CSR space (AM=2F). Section 2.3.12 of VME64
- 512kB per module located in system space by "BAR" (base address register, A23...A19)
- BAR must be initialized (e.g. autoslot-id)
- CSR's start from top address
- CR's start from bottom
- Middle part is user CR/CSR space
- Must be minimal D08 access.
- big-endian (msb of multibyte object at lowest address)

VME64 minimum register definition

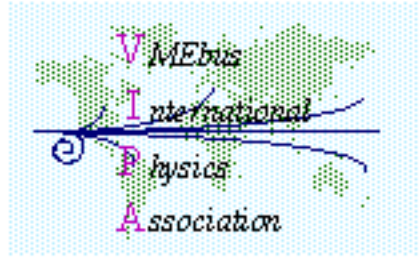
- Bytes every 4th address (byte ROM)
  - Unused bytes must read 0x00.
- CSRs 3 bytes
  - BAR
  - bit set for SYSFail and Reset control
  - bit clear " " " "

VME64 minimal register definition (2)

- CRs

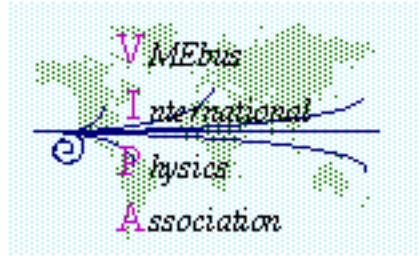
	bytes
– ROM checksum and length	1+3
– data-access width for CR and CSR	1+1
– spaceID (value=1 for VME64)	1
– "CR" ascii	2
– manufacturer ID	3
– board ID	4
– board revision ID	4
– program ID	1
– pointer to printable string	3
	24 bytes.

VME64x CR/CSR



- Chapter 10 of VME64x
- BAR loaded with geographic address (GA) at power-up
  - For backward compatibility with VME,VM64, sense circuitry can detect absence of GA (=31) and use switch settings instead
  - Amnesia address =30 in case of corrupt GA
- User Configuration RAM (CRAM)
  - semi-static, permanent information
- Begin and end pointers to user CR/CSR/CRAM sections
  - framing
  - makes decoding easier
- Many more optional but defined registers

VME64x CR/CSR (2)

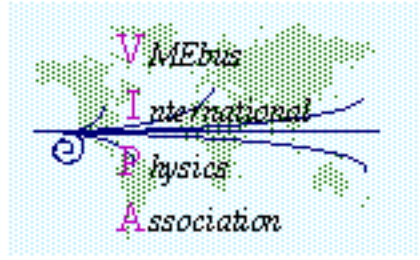


- CR additions (555 bytes)
  - **master/slave characteristics**
    - unaligned transfer, RMW, Retry, P2, ETL, address onl.
  - **Interrupt handler capability**
  - **Interrupter capability**
  - **Pointers to serial number**
  - **Master capability (AMs, XAMs, Data access width)**

VME64x CR/CSR (3)

- **8 Slave 'functions' definitions**
  - Function = slave address space decoder.
  - 'Plug&Play' alternative to jumpers/switches
  - defined by 4 registers in CR
    - DAW = data access width (D8, D16, D32, ...)
    - AM and XAM codes
    - ADEM = address bit mask (→ size)
  - and 1 r/w register in CSR
    - ADER = address decoder compare value.
  - This mechanism also called
  - 'address relocation'

Address Relocation example



- A32/D32 BLT (AM=0b) at offset 0x42220000
  - ADEM = 0xFFFE0000
  - ADER = 0x4222002C

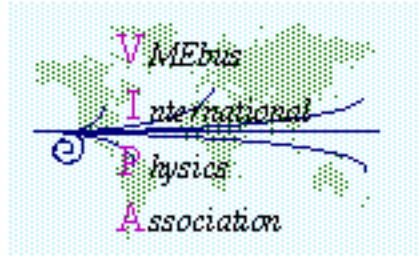
VME64x CR/CSR (4)

- CSR 's additions (216 bytes)
  - **Bit set/clear register extended**
    - BERR*, enable module 'function', CRAM semaphore
  - **User bit set/clear registers**
    - 8 user-defined control bits
  - **8 ADER's**

VME64xP CR/CSR

- Chapter 3 of VME64xP
- CR/CSR space is mandatory
  - CR:
    - some VME64x defined CR must be inplemented: BAR, Manuf ID, board ID, serial nb
    - other unused VME64x defined CR's must read as 0
    - new VME64xP defined CR:
      - VME64xP capability; byte count, self-test register, MCST, CBLT, user defined
  - CSR:
    - Address relocation recommended
    - Transfer Byte count register
    - 2 csr's for MCST ,CBLT support

Summary



- 'Layered' definition, keeping compatibility across VME64, x, xP
- CR layout aimed for byte-PROM (every fourth byte)
- CR space is bells & whistles: who cares, it's all in a huge PROM . . .
- CSRs require slave controller COTS (ADERs, . . .)
- Benefits
  - Uniform practice for information (ID, interrupt, . .)
  - Plug & Play, no jumpers (capabilities, slave functions, . . .)
- Java-tool for (de-)compiling CR-ROM?