Draft Standard for a Common Mezzanine Card Family: CMC

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Microprocessor & Microcomputer Standards Committee (MMSC)
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Abstract: This draft standard defines the mechanics of a common mezzanine card family. Mezzanine cards designed to this draft standard can be used interchangeably on VME, VME64 & VME64x boards, CompactPCI boards, Multibus I boards, Multibus II boards, desktop computers, portable computers, servers and other similar types of applications. Mezzanine cards can provide modular front panel I/O, backplane I/O or general function expansion or a combination for host computers. Single wide mezzanine cards are 75 mm wide by 150 mm deep by 8.2 mm high.

Keywords: Backplane I/O, Bezel, Board, Card, CompactPCI, Face Plate, Front Panel I/O, Host Computer, I/O, Local Bus, Metric, Mezzanine, Module, Modular I/O, Multibus, PCI, VME, VME64, VME64x or VMEbus

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Change Bars
All paragraphs changed in this draft (2.4a) from draft 2.3 are marked with a change bar on the right side of the paragraph. Any table entry that was changed will have a thicker vertical line on the right side of changed entry. Any figure that was changed will have a charge bar on the right side of the figure title. Only one change was made to draft 2.4a over draft 2.4: The last sentence in paragraph 6.4.3 was deleted, due to negative comments from RevCom.

Introduction
(This introduction is not part of this Draft Standard, Draft Standard for a Common Mezzanine Card Family: CMC.)

The major goal of this draft standard is to provide the mechanics of a mezzanine card family that can be deployed on a variety of different host computer platforms. These mezzanine cards can be use to provide front panel I/O, rear panel I/O, additional local host functions or a combination of the three. The mezzanine card's local bus can be PCI, SBus or other local buses as they are developed in the future. The second goal of this draft standard is to only have one mezzanine card mechanical definition for a specific type of local bus rather than having multiple mechanical implementations as has happened in the past. Multiple mechanical implementations fragments the market and destroys economy of scale for manufacturing, engineering, sales and marketing. A single mechanical definition builds larger markets with many more unique functions being provided for the multitude of user applications, and at a lower price. Both the suppliers and users win by enjoying the benefits of a larger unified market.

SBus Historical: In 1993 when the effort to develop a mezzanine card standard was started, there seemed to be a market need to shrink the SBus (IEEE 1496-1993) mechanical form factor such that it would fit in a single VME board slot. (SBus cards are 20.32 mm high and take up a second VME slot when attached to a VME host board.) A SBus Mezzanine Card (SMC) child draft standard was developed and made it into the sponsor ballot phase. [See Section 1.5 for definition of child standard.] This draft standard, P1386.2 was titled "Draft Standard Physical and Environmental Layers for SBus: SMC". Due to the overwhelming popularity of the PCI local bus, no market interest developed for the single slot SBus version, SMC. P1386.2 was dropped as a proposed IEEE standard in the summer of 1996.

Futurebus+ Historical: In 1993 most of the core Futurebus+ (IEEE 896.x) standards had been completed. At that time there seemed to be a reasonable market interest in the Futurebus+ architecture. The mechanics of placing mezzanine cards on Futurebus+ modules was included in the core P1386 mechanical definition, draft 2.0. Unfortunately, the market for Futurebus+ never developed. During this standard's sponsor ballot phase, it was decided to remove all references to Futurebus+ in both the P1386 and P1386.1 draft standards. Since the extended CMC form factor (250 mm deep) version was specified mainly for the Futurebus+ applications,

it was also dropped from both the P1386 and P1386.1 draft standards. As a result, only two CMC form factors are defined, single width and double width.

CompactPCI Historical: After the first sponsor ballot (April, 1995) a new bus architecture was introduced to the market that rapidly gained large market interest. CompactPCI transformed the PCI local bus into a backplane bus with a maximum of eight slots. CompactPCI board, backplane and subrack mechanics are the same as VME64x, except for the backplane connectors. All the board and subrack mechanics defined for the VME64x architecture applies directly to CompactPCI. VME64x provides 205 and CompactPCI provides 315 user defined I/O pins through the backplane. The PICMG (PCI Industrial Computers Manufacturers Group) is responsible for the promotion and maintenance of the CompactPCI specifications.

Routing of PMC I/O to the rear of CompactPCI boards is defined and controlled by PICMG. Surf to www.picmg.com for information on how to get copies of these detailed specifications.

Special thanks are due to Dave Moore, original P1386 Working Group Draft Editor, for the generation of the many drafts, to Eike Waltz for the key mechanical designs of the CMC and to Dave Rios on the connector design. Heinz Horstmeier, Cliff Lupien, Harry Parkinson, Rick Spratt, and Chau Pham are also to be thanked for their contribution to development of this proposed standard.

Wayne Fischer, Chair & Draft Editor

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Draft Standard for a Common Mezzanine Card Family: CMC

1. Overview

1.1 Scope

This draft standard defines the mechanics for a common set of slim mezzanine cards that can be used on VME, VME64 & VME64x boards, CompactPCI boards, Multibus I boards, Multibus II boards, desktop computers, portable computers, servers and other similar computer applications. Mezzanine cards based on this draft standard can be used to provide modular front panel I/O, backplane I/O or general function expansion for the host computer.

1.2 Purpose

The majority of the popular RISC & CISC microprocessors are using the same logical and electrical layer for their high speed local bus. These same processors are being incorporated onto VME64x boards, CompactPCI boards, Multibus I & II boards, desktop computers, portable computers, servers and other types of computer systems. There is a large market need for modular I/O and modular local function expansion via slim mezzanine cards mounted parallel above these host computer's board.

This draft standard defines the mezzanine card mechanics for these types of applications. This mechanical definition is based on IEEE 1301.4-1996[10].

1.3 General Arrangement

Mezzanine cards are intended to be used where slim parallel card mounting is required such as in embedded single board computers, desktop computers, portable computers and servers. Figure 1-1 illustrates a single size and a double size mezzanine card defined by this draft standard.

Typical single and double size CMCs on VME64x are illustrated in Figure 1-2. Implementation of CMCs on CompactPCI and Multibus II boards is similar to 6U VME64x except that Multibus II boards are 220 mm deep and CompactPCI uses a 2 mm connector system. CMCs can also be used on 3U VME64x and CompactPCI boards.

Multibus I boards don't use front panels. I/O is via the top edge of the board. Figure 1-3 illustrates a single CMC and two single CMCs on a Multibus I board.

The size and shape of desktop computers, portable computers, servers and other similar types of computers varies considerably, depending on specific target markets and associated needs. Figure 1-4 illustrates how a CMC could be mounted inside a desktop or portable computer host. The I/O panel arrangement would be similar to one already illustrated.

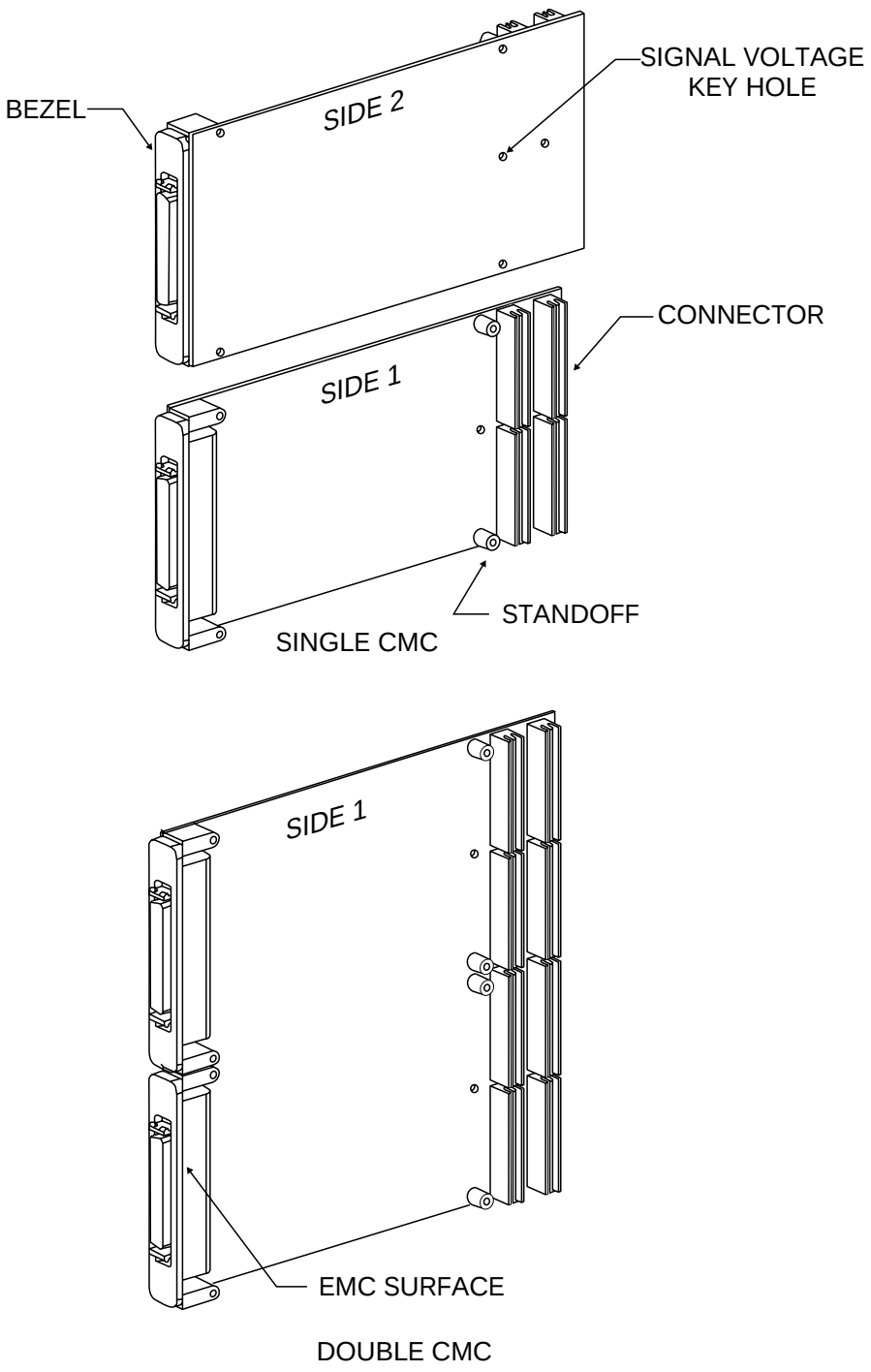

Figure 1-1
Typical Single and Double CMC

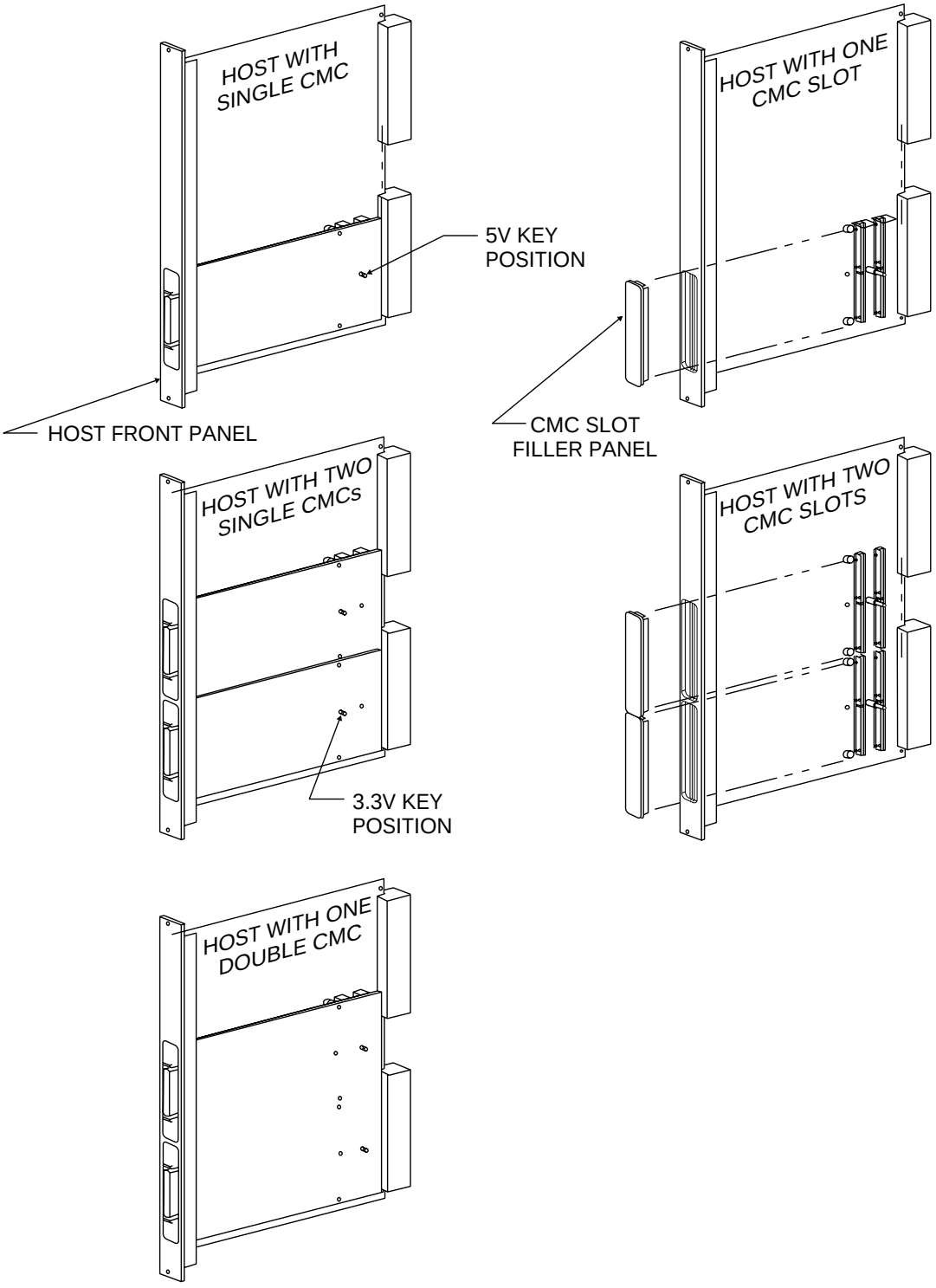

Figure 1-2
Typical Single and Double CMC on a 6U VME64x Host

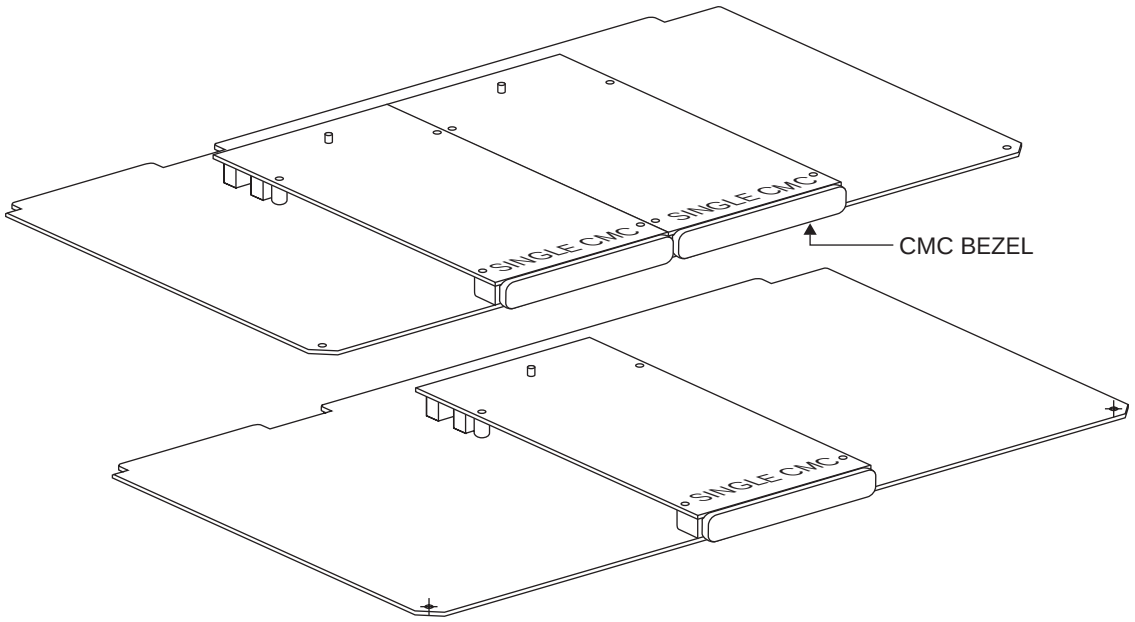

Figure 1-3
Typical One or Two Single CMCs on Multibus I Host

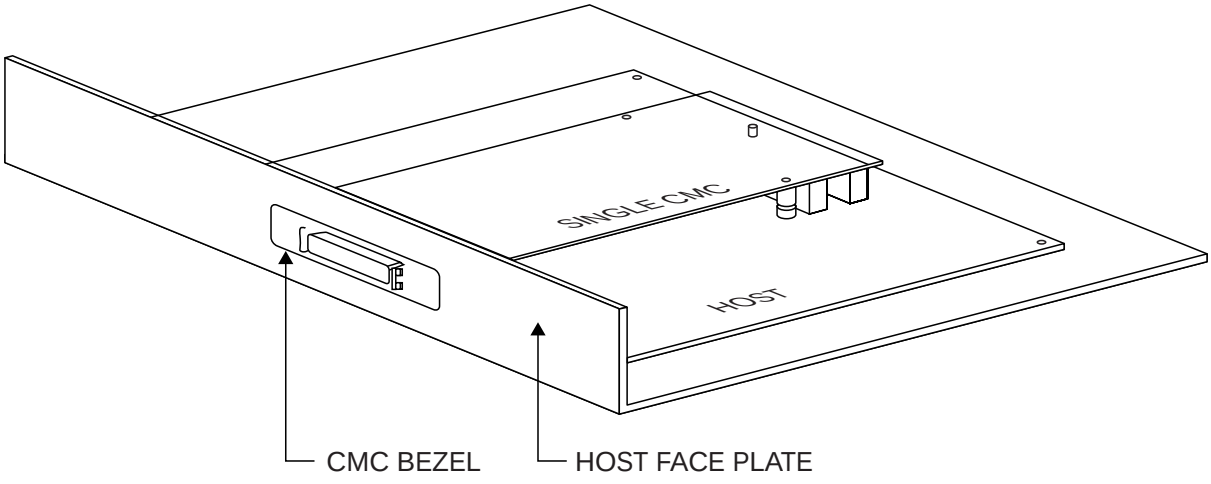

Figure 1-4 Typical CMC in a
Desktop or Portable Computer Host

1.4 Theory of Operation and Usage

CMCs are designed to be plugged into a slot, above the host's printed circuit board. The host may place low height components under the mezzanine card for additional functionality. The host is to provide one or more slot opening(s) into which the mezzanine card(s) are plugged. The host slot opening provides mechanical support as well as EMI shielding. For maximum utilization of component space, the mezzanine card is typically placed such that the major component side (side one) of the mezzanine card faces the major component side (side one) of the host computer's main board.

The local bus interface to the host computer is provided via one or more connectors between the mezzanine card and the host board. These connectors reside on the rear of the mezzanine card.

I/O off the mezzanine card can be via the front panel (bezel) or via one or more of the mezzanine card connectors. If the I/O is through the mezzanine card connector, the I/O is generally routed to the host's computer's backplane, such as is commonly done on VME64x, CompactPCI, Multibus I & II based computer systems.

1.5 Parent-Child Standard

This standard acts as a parent standard to one or more child standards. At the time this standard was developed and approved, one child standard was developed and approved at the same time. This is the P1386.1, Draft Standard for Physical and Environmental Layers for PCI Mezzanine Cards: PMC. The P1386.1 standard provides the specific connector pin assignment of the PCI local bus, as it is routed on to the mezzanine card. In the future, additional child standards can be developed that use the basic mechanical definition (from this standard) but have different local buses.

Note that the P1386.1 (PMC) standard references other standards or specifications for the definition of the local bus's logical and electrical layers.

1.6 Conformance

A vendor of mezzanine cards or host computers (or host peripherals) may claim compliance with this standard only when the complete mechanical interface is met.

1.7 Dimensions

All dimensions in this draft standard are in millimeters (mm) unless otherwise specified. Drawings are not to scale. First angle projection has been used throughout this draft standard.

1.8 Coordinate Dimensions

1301.4-1996[10] brackets correspond to those of the references in Section 2. This defines the actual dimensions of a 25 mm metric equipment practice. These actual dimensions are derived from coordination dimensions using the principle of boundary and axis references illustrated in IEEE Std 1301-1991[9] and IEC 917-2-1[3].

Overall dimensions and internal subdivisions are determined by using different increments or mounting pitches (mp1 = 25 mm, mp2 = 5 mm, mp3 = 2.5 mm, mp4 = 0.5 mm and mp5 = 0.05 mm). These mounting pitches have been used to derive the key dimensions given in this

standard. They are also used when extending this standard with additional dimensions (where such extensions are permitted) and when alternative positions of piece parts are described. (In such cases, it is obvious that the relationships between involved dimensions shall be maintained.)

2. References

The following publications are used in conjunction with this standard:

[1] EIA 700 AAAB, 1 Millimeter, Two-Part Connector for Use with Printed Boards are available from Global Engineering 1990 M Street NW, Suite 400, Washington, DC 20036, USA.

[2] IEC 48D (Secretariat) 76, Draft for Part 1: Mechanical aspects/climatic tests for cabinets, racks and subracks for the IEC 917- and IEC 297- Series 33EC Sales Department, Case Postale 131, 3 rue de Varembe, CH-1211, Geneve 20, Switzerland/Suisse. IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036

[3] IEC 917-2-1, Modular order for the development of mechanical structures for electronic equipment practices.

[4] IEEE 796-1983, IEEE Standard Microcomputer System Bus (Multibus I). IEEE standards are available from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA, www.ieee.org

[5] IEEE 1101.1-1998, Mechanical Core Specification for Microcomputers using IEC 603-2 Connectors.

[6] IEEE 1101.10-1996, Specifications for Additional Mechanical Specifications using the IEEE 1101.1 Equipment Practice.

[7] IEEE 1156.1-1993, IEEE Standard for Microcomputer Environment Specification for Computer Modules.

[8] IEEE 1296-1994 IEEE Standard for a High-Performance Synchronous 32-Bit Bus: MULTIBUS II.

[9] IEEE 1301-1991 IEEE Standard for a Metric Equipment Practice for Microcomputers-Coordination Document.

[10] IEEE 1301.4-1996 IEEE Standard for a Metric Equipment Practice for Microcomputers-Coordination Document for Mezzanine Cards.

[11] ANSI/VITA 1-1994 VME64 Standard. www.vita.com

[12] ANSI/VITA 1.1-1997 VME64x Standard.

[13] PICMG 2.0, R3.0 CompactPCI Specification. www.picmg.com

[14] ANSI/IEEE 1014-1987 IEEE Standard for A Versatile Backplane Bus: VMEbus

[15] EN55022-1998 Information Technology Equipment. Limits and Methods of Measurement of Radio Disturbance Characteristics, www.itic.org

[16] EN55024 Information Technology Equipment. Immunity Characteristics. Limits and Methods of Measurement, www.itic.org

[17] EN50082-1 Information Technology Equipment. Part 1: Residential, Commercial & Light Industry Electromagnetic Compatibility, www.itic.org

[18] FCC Part 15 Federal Communication Commission, Equipment Identification Rules. www.fcc.gov

[19] EN300 386-2 *(title to be added during final IEEE editing phase)* www.itic.org

[20] Bellcore GR-1089-CORE Electromagnetic Compatability & Electrical Safety – Generic Criteria for Network Telecomm

When any of the above specifications are superseded by an approved revision, that revision shall apply.

2.1 Trademarks

The following names used within this draft standard are trademarked:

MULTIBUS is a registered trademark of Intel Corporation.

PICMG and CompactPCI are registered trademarks of the PCI Industrial Computers Manufacturers Group.

2.2 Relationship between VME, VMEbus, VME64, VME64x and CompactPCI

The original VME specification is specified by ANSI/IEEE 1014-1987[14] VME Standard, "IEEE Standard for a Versatile Backplane Bus: VMEbus". A second generation VME standard was developed that expanded VME to a 64 bit address and data width bus architecture. It was developed by the VITA Standards Organization (VSO) and is called ANSI/VITA 1-1994[11], VME64 Standard. All of the original IEEE VME standard definition was incorporated in the VME64 standard. A third generation VME standard was develop called ANSI/VITA 1.1-1997[12], VME64 Extensions (VME64x) Standard. The standard added a variety of additional features, including an expanded 160 pin connector, a center 95 pin 2 mm connector, an EMC U shaped front panel, ESD protection, +3.3V & 48 volt power, front panel keying, etc.

All the mechanical features defined in the VME64x standard are utilized in the CompactPCI Specification[13]. Mechanical placement of the CMCs on VME64x and CompactPCI 3U and 6U boards is exactly the same. The only difference is routing of the CMC's I/O through the rear backplane connectors. CMCs can be used on VME and VME64 boards with flat front panels. There is less mechanical flex strength in the flat front panels versus U shaped front panels. The preference should be to use the U shaped front panels, in all Eurocard type applications.

The terms "VME" and "VMEbus" mean the same thing and are used interchangeable.

3. Definitions, Abbreviations and Terminology

3.1 Special Word Usage

shall, A key word indicating a mandatory requirement. Designers shall implement specific mandatory requirements to ensure interchangeably and to claim conformance with the standard. This key word is used interchangeably with the phrase "is required".

should, A key word indicating flexibility of choice with a strongly preferred implementation. This key word is used interchangeably with the phrase "is recommended.

may, A key word indicating flexibility of choice with no implied preference. This key word is used interchangeably with the phrase "is optional".

3.2 Definitions

coordination dimension. A reference dimension used to coordinate mechanical interfaces. This is not a manufacturing dimension with a tolerance.

mezzanine card. An add-on printed circuit board (PCB) which is mounted parallel to a host computer board. Note that some applications use the “module” word instead of the “board” word, which have the same meaning.

reference plane. A theoretical plane, not having thickness or tolerance, used to separate space. See IEEE 1101.1-1998 [5].

true position. Defined as some point on a card's PCB, that is used by the assembly equipment for the reference positioning of a set of components.

3.3 Abbreviations

The following abbreviations are used extensively in this draft standard:

CMC	Common Mezzanine Card
H	height nomenclature
I/O	input/output
Jn	Connector receptacle number
mm	millimeter
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
Pn	Connector plug number

3.4 Dimensional Nomenclature Heights, Width, and Depth

Following is a list identifying abbreviations and a description of height dimensional nomenclature used in this draft standard:

Nom	**Description**
H1	CMC side 1 component height
H2	CMC side 2 component height
Hp	CMC plug seating plane height
Hs	CMC standoff height and reference plane height

There are no **width** and **depth** dimensional nomenclatures used in this draft standard.

4. Mezzanine Card Mechanics

This chapter defines the mechanical dimensions for mezzanine cards. The host mezzanine card slot mechanics are defined in the next chapter.

4.1 CMC Size Designations and Sizes

Two different mezzanine card sizes are defined. These two sizes are listed in Table 4-1. The designation of each card size is given in the first column.

Table 4-1
CMC PWB Size Designations and Dimensions

Designation	Width	Depth
Single	74.0	149.0
Double	149.0	149.0

Note that CMC's envelope boundaries are designed on a grid structure, where the basic increment of the grid is 25 mm. The width increment of CMCs is 75 mm. When two CMCs are placed next to each other, there is a 1 mm gap between each CMC.

The depth of CMCs is 149 mm. Should other mezzanine cards be used in conjunction with one or more CMCs, there will be a 1 mm gap between the edges of two single CMCs.

If the reader needs more understanding of this grid structure and wants to know how it ties into the international metric measurement systems, the reader should obtain a copy of (IEEE) 1301.4-1996 [10] Standard.

4.2 CMC Envelope

A key concept in this standard is the CMC envelope which defines a space that may be occupied by the CMC PCB, associated electronic components and required cooling gap. The total CMC envelope space is divided into two parts, the component envelope and the I/O envelope. The envelope for a single CMC is shown in Figure 4-1. The component envelope maximum height shall be 8.2 mm and 13.5 mm for the I/O envelope. The maximum depth of the I/O envelope shall be 31.0 mm.

The component envelope is where electronic components (such ICs, chips, devices, resistors, capacitors, etc. plus the printed circuit board) may be placed. No component is allowed to protrude through this envelope, except the CMC connectors, standoffs and bezel retention screws. PCB warpage during the manufacturing process shall be included for calculating and measuring maximum component heights so as not to protrude through this envelope.

The I/O envelope (area) shall be used for mounting of I/O connectors on the CMC bezel. In some applications, no I/O connectors are used, therefore this envelope may then be used for mounting of components. Larger components may also be placed in this envelope. A connector or component of any kind shall not protrude outside this specified envelope. The only exception is the CMC bezel and I/O connectors mounted on the bezel which protrude beyond the face of the bezel. No limit is defined for the length of this protrusion. See Figure 4-6 for further mechanical details on the I/O envelope of the mezzanine card.

4.3 CMC Dimensions

Figures 4-2 and 4-3, show the mechanical dimensions that shall be used for both CMC sizes. The rest of the mechanics are found on the single or double CMC dimensions. Note that the standoff hole size is not defined. The size of these holes depends on how the standoffs are permanently attached to the CMC during assembly.

4.4 Voltage Keying

Many of the new local buses can operate at one of two different voltage levels. For these types of applications, voltage keying holes are provided on the mezzanine cards. The two voltage are 5V and 3.3V. If the mezzanine card's local bus operates on the 5V signaling level, it shall provide a 5V keying hole. If the mezzanine card's local bus operates on the 3.3V signaling level, it shall provide a 3.3V keying hole. If both voltages can be supported, then both holes shall be provided. See Figures 4-2 and 4-3 for location of these holes. The associated keying pins are defined in the next chapter. The host is to provide the keys.

4.5 Connector Pads and Labeling

Figure 4-4 shows the connector pads layout that shall be used for each connector placed on a CMC. The labeling of each pin within each connector shall also follow the pin numbering scheme shown in Figure 4-4.

Depending on the functionality of the CMC, anywhere from one to four connectors may be used, and in any combination. Recommendations as to which combinations are used are left to the child standards which use this standard for the mechanical card definition.

4.6 CMC Connector

All CMC connectors shall use the EIA E700 AAAB connector as defined by the EIA standard in reference [1]. These connectors shall be referred to as the plug, or "Pn" connector. For single wide CMCs, the connectors shall be labeled P11 through P14. When double wide CMCs are used, the connector numbers shall be P11 through P14 and P21 through P24. See Figures 4-2 and 4-3. If a CMC does not use all of the connectors, this space is open to be utilized by additional components. A special caution is noted as a CMC with connectors missing could be plugged in to a host with all connectors mounted, thereby making restricting component heights in the connector area mandatory. For CMCs that do place components, other than connectors in the connector area, these components shall not exceed a height of 4.0 mm.

4.7 CMC Connector Assembled on a CMC

Assembly of all the CMC connectors on a mezzanine card shall be within +/- 0.14 mm of true position (TP). TP is defined as some point on a mezzanine card's PCB, near the connector(s), that is used by the assembly equipment for the reference positioning of the connector(s) prior to soldering.

The angular mis-alignment of any connector shall not exceed 1.5 degrees, or shall not exceed 0.94 mm of perpendicular mis-placement from one end of the connector to the other end of the connector (long dimension). The angular mis-alignment of any connector across the width (short dimension) shall not exceed 1.5 degrees, or not exceed .16 mm of perpendicular mis-alignment.

The solder thickness variation between the connector contacts and the solder coated surfaces on the mezzanine card shall not exceed 0.1 mm. Excessive build up of solder under the connector contacts will cause the connector to be mounted too high such that when assembled on a host computer, the plug and receptacle connector seating surface will touch and push against each other with excessive force.

4.8 CMC Component Heights

The referenced size CMC is designed to accommodate components up to 4.7 mm in height on side 1. On side 2 the component height can be up to 3.5 mm minus the PCB thickness. See Figure 4-6 for a side view of CMC component area.

Note that warpage of the PCB shall be included in the component height on both sides.

In some applications, it may be necessary to use taller or shorter components on a CMC. In these situations more height is needed for the component vertical space.

The CMC is designed to provide for this flexibility. The CMC's PCB may be moved up or down for this added height, depending on whether the added height is needed on side 1 or side 2. Table 4-2 shows the height relationship.

Designers must realize that if one side's height is increased, the other side's height is decreased accordingly, since the CMC envelope can not be changed.

Note that special components which are not electrically isolated (have conductive top surfaces) from the PCB's power and ground planes shall be shorter in height and shall not protrude through the special heights listed in Table 4-2. This additional margin is 0.7 mm. Conductive surface components are allowed in the designated I/O area because the host module provides a restricted area which allows no conductive traces or vias.

Table 4-2
Relationship Between Stacking, Standoff, Component and Plug Seating Heights

Standoff and Stacking Height (Hs +/- 0.10) Figure 4-5	Side 1 Comp. Area Height (H1) Figure 4-6	Side 2 Comp. Area Height (H2) Figure 4-6	Special** Component Height on Side 1	Plug Seating Height (Hp) Figure 4-5
8.00	2.70	5.50	2.00	2.30
9.00	3.70	4.50	3.00	3.30
10.00*	4.70*	3.50*	4.00*	4.30*
11.00	5.70	2.50	5.00	5.30

* CMC reference plane height used for the nominal mezzanine card height dimensions..
** Components with conductive top surfaces are limited to these component heights.

4.9 CMC Connector and Standoff Heights

The referenced "*" CMC side 1 surface is designed to be placed 10 mm from the host side 1 surface. Standoffs are used to maintain the spacing between the CMC and the host, and to provide mechanical rigidity. The connectors are designed to be fully mated but not bottoming at the seating surfaces when assembled to a host.

Note that the CMC side 1 reference plane may be the top surface of the solder coated surfaces for the connector contacts. It is recommended that solder coated surfaces be used under the

standoffs and CMC bezel for additional strength and consistency for maintaining proper spacing between the mezzanine card and the host.

Whenever the PCB's vertical position is changed, the corresponding standoff and connector's seating surface shall also be changed. The CMC envelope's position above the host shall remain fixed. Table 4-2 lists the relationship (change in dimensions) between the plug seating height and the standoff's height as the side 1 and side 2 component area heights are increased or decreased. Effectively the CMC PCB is moved up or down, respectively.

Figure 4-7 illustrates the CMC PCB height variation above the host.

The mezzanine stand-off shall be an internal part that is permanently attached to the mezzanine card. The standoff shall also provide internal threads for a threaded fastener from the host side. The fasteners for the standoffs shall be provided by the CMC vendor. Standoff material is not defined by this specification.

The mezzanine card standoffs may optionally be soldered or riveted to the CMC PCB.

4.10 CMC Bezel

The bezel of a CMC has two basic parts, the bezel, and the EMC gasket.

Each CMC shall be designed to accommodate a bezel. The main function of the bezel is for mounting of front panel I/O connectors and/or special indicators and switches. Since standard size bezels are used, the CMC can fit into any host which provides a CMC slot. Figure 4-8, shows the mechanical design of the CMC bezel.

The two legs on the bezel also provide the standoffs for the front portion of the mezzanine card. The height of these legs shall be the same as the two standoffs used near the CMC connectors.

Should the CMC PCB be moved up or down within the CMC envelope, then the bezel leg height shall be adjusted accordingly. See Table 4-2 for this relationship.

The center horizontal line of the CMC bezel shall always be 5.5 mm above the host side 1 surface, for the 10 mm stacking height. See Figures 4-6 for this illustration. Note that if the CMC PCB is moved up or down, the CMC bezel's center line does not move. The bezel always maintains the same relationship with the host's side 1 surface and host front panel (face plate).

4.11 CMC Test Dimensions

It is very important that fully assembled CMCs be measured to ensure that when the CMC is plugged into a host's CMC slot, it will properly match. There are three critical dimensions that shall be measured to verify that a CMC will fit properly in a host computer's CMC slot.

The first critical dimension is the distance between rear connectors (0.00 reference) and the CMC bezel center line. When a CMC is plugged into the host computer's CMC slot, the CMC bezel should be aligned with the host computer's CMC slot opening. Due to tolerance build up, this will not perfectly match. The actual mismatch may be as much as +/- 0.3 mm. See Figure 4-9.

The second critical dimension is the perpendicular center line of the CMC connector to the perpendicular center line of the CMC bezel. This is specified in Figure 4-9.

The third critical dimension is the vertical height of the CMC bezel and standoffs off the CMC reference plane. The center of the bezel shall be within the tolerance specified in Figure 4-6 and the standoffs with the numbers given in Table 4-2.

4.12 I/O Capability

I/O capability may be via the CMC front panel, backplane I/O via host, or both.

For I/O through the host's backplane, such as VME64x, CompactPCI, or Multibus I, Multibus II, one or more of the CMC connectors may be assigned for this capability. See chapter 6 of this draft standard for the required mappings.

4.13 Power Consumption and Dissipation

The power drawn from the host by each mezzanine card as well as heat dissipated by the facing host computer's board shall have a maximum limit. Host computer designers can then design for the worst case in both power draw as well as removal of heat generated by the mezzanine card. Table 4-3 lists the maximum power consumption and dissipation for each of the mezzanine card sizes. Since the mezzanine card side 1 faces the host, the power dissipated on side 1 is also limited to minimize heat build up between the host and the mezzanine card.

Table 4-3
CMC Maximum Power Consumption and Heat Dissipation (in Watts)

	Single	Double
Side 1	6.0	12.0
Side 1 + Side 2	7.5	15.0

Manufacturers that supply mezzanine cards to the open market shall provide the following information on each mezzanine card:

- 5V current drawn, peak and average
- 3.3V current drawn, peak and average
- Average power dissipated on side 1
- Average power dissipated on side 2
- Percent of side 1 area, side view, that is not occupied by components
- Percent of side 2 area, side view, that is not occupied by components

For some applications, users may need to calculate the amount of air flow that can flow across a mezzanine card for proper cooling purposes.

Note that VITA Standards Organization had defined an extended specification for processors CMC and PMCs. Go to www.vita.com for further detail.

4.14 Ground Connections

The CMC front panel bezel shall be electrically isolated from mezzanine card circuit ground to prevent ground loop problems. Boards should provide a minimum of 50 V DC and 100 kOhms of isolation between the CMC front panel bezel. More isolation may be required depending on system requirements.

The required standoffs, which are attached to the mezzanine card near the P11 and P13 connectors, shall be tied to the mezzanine card's circuit ground so that they do not float and create unwanted antennas. All keying holes shall remain electrically isolated from the mezzanine card's circuit ground.

4.15 Electromagnetic Compatibility

CMC boards shall meet the standards of the latest harmonized versions of the following specifications. CMC boards should meet class B emissions and a minimum of performance criteria B for immunity. For ITE (Information Technology Equipment), use EN50022-1998[15] for emissions and for immunity use EN55024[16] and EN50082-1[17]. For products used in the United States refer to FCC Part 15[18] for emission requirements above 1GHz. For telecom applications, use EN300386-2[19] and Bellcore GR1089-CORE[20].

Functional mezzanine cards with I/O off the front panel may be designed and manufactured to meet the higher EMC performance levels as well as meet other national and international EMC standards, such as those specific to telecommunications, so long as the minimum requirements specified in this standard are met.

It is recommended that mezzanine card vendors list any EMC standards, and to which level(s) that are met in the product specifications. It is also recommended that any test results should be published in the same product specifications.

4.16 Shock and Vibration

All mezzanine cards installed in a host shall at a minimum meet performance level V.2 of the shock and vibration requirements specified in reference [2].

Mezzanine card suppliers may design and manufacture mezzanine cards to meet higher shock and vibration performance levels as well as meet other national and international shock and vibration standards, so long as the minimum requirements specified in this standard are met.

It is recommended that mezzanine card vendors list the shock and vibration standards, and to which level(s) that are met in the product specifications. It is also recommended that any test results should be published in the same product specifications.

4.17 Environmental

Mezzanine cards may be designed and manufactured to meet the higher environmental levels as specified in the following two sections, as well as meet other national and international environmental standards, such as those specific to telecommunications, so long as the minimum requirements specified in this standard are met.

It is recommended that mezzanine card vendors list the environmental standards, and to which level(s) that are meet in the product specifications. It is also recommended that any test results should be published in the same product specifications.

4.17.1 Mechanical

All mezzanine cards shall at a minimum meet performance level C.1 of the climatic requirements specified in reference [2], but at 85% air humidity. They shall also at a minimum meet performance level I.1 of the industrial atmosphere requirements specified in reference [2].

4.17.2 Electronic Components

The electronic components on all mezzanine cards shall at a minimum meet performance level 4 as specified in reference [2]. This reference specifies the temperature, humidity and other environmental requirements.

4.18 MTBF

Mezzanine card vendors should state the expected MTBF (mean-time-between-failures) of each mezzanine card for a specific operating environment, and shall state what method was used to calculate the MTBF number(s).

4.19 ESD Design

Providing for ESD protection may be difficult in some of the mezzanine card's electronic design. Standoffs are required to be tied to the mezzanine card's circuit ground. It is recommended that mezzanine card handlers (the person who installs a CMC into a host) first touch one of the standoffs to bleed off any electrical static energy, should it be present. Placing a small ground trace around the perimeter of the mezzanine card may also be used to bleed off any potential static energy, if the handler first touches the mezzanine card's edge when picking it up.

4.20 ESD Kit

It is recommended that mezzanine card vendors supply an ESD (electro-static discharge) kit with each mezzanine card. This kit is essentially a grounding strap and a wire that connects the mezzanine card handler to the host's chassis ground prior to installing a mezzanine card in to the host. Should any static electricity be present, it will be discharged and thereby prevent any possible static discharge damage to the host and/or mezzanine card.

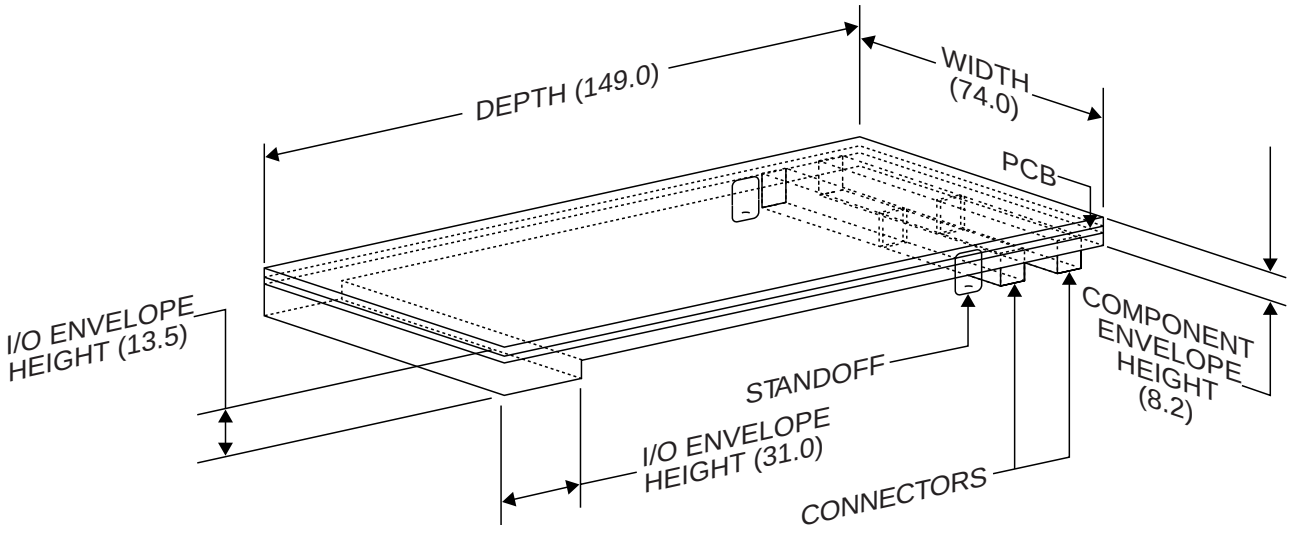

Figure 4-1
Single Size CMC Envelope
(Front Panel not shown)

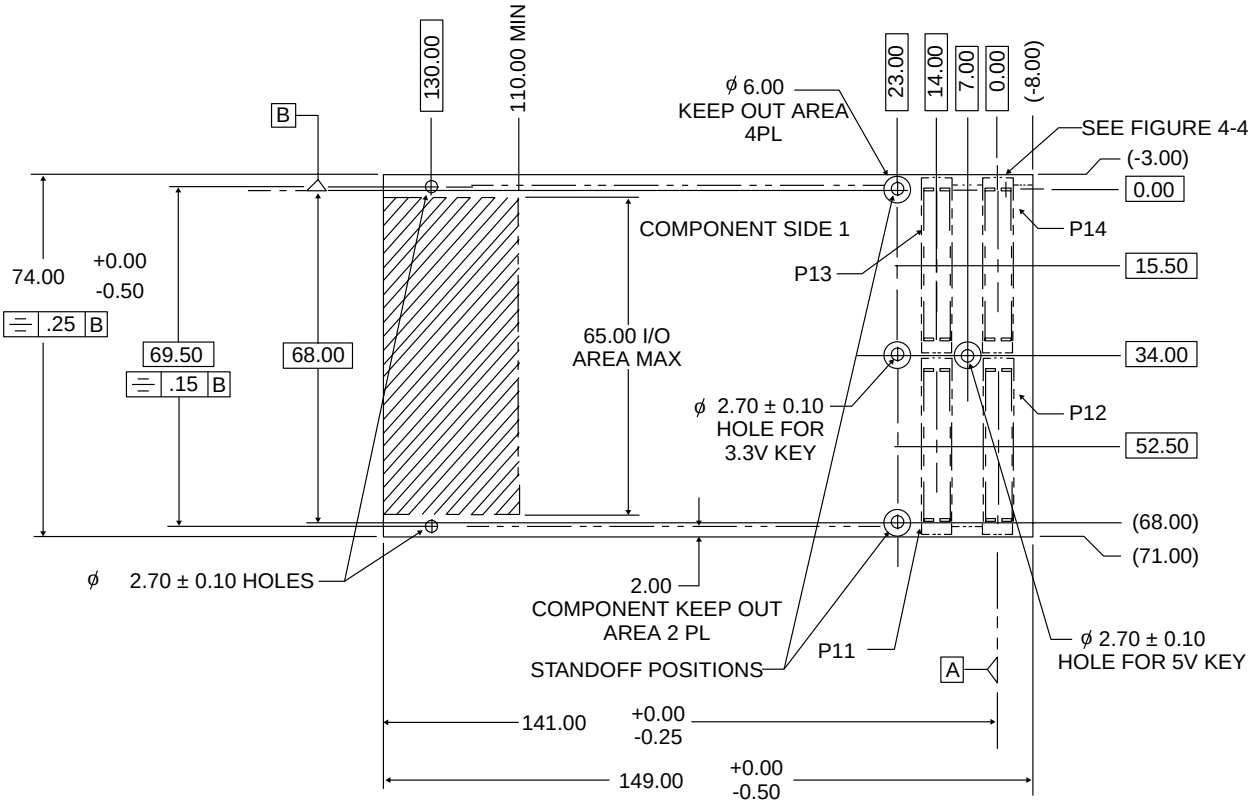

Figure 4-2
Single CMC

Note: Basic Dimensions are to be true position within .15 mm of Datum A and Datum B for Figures 4-2 and 4-3.

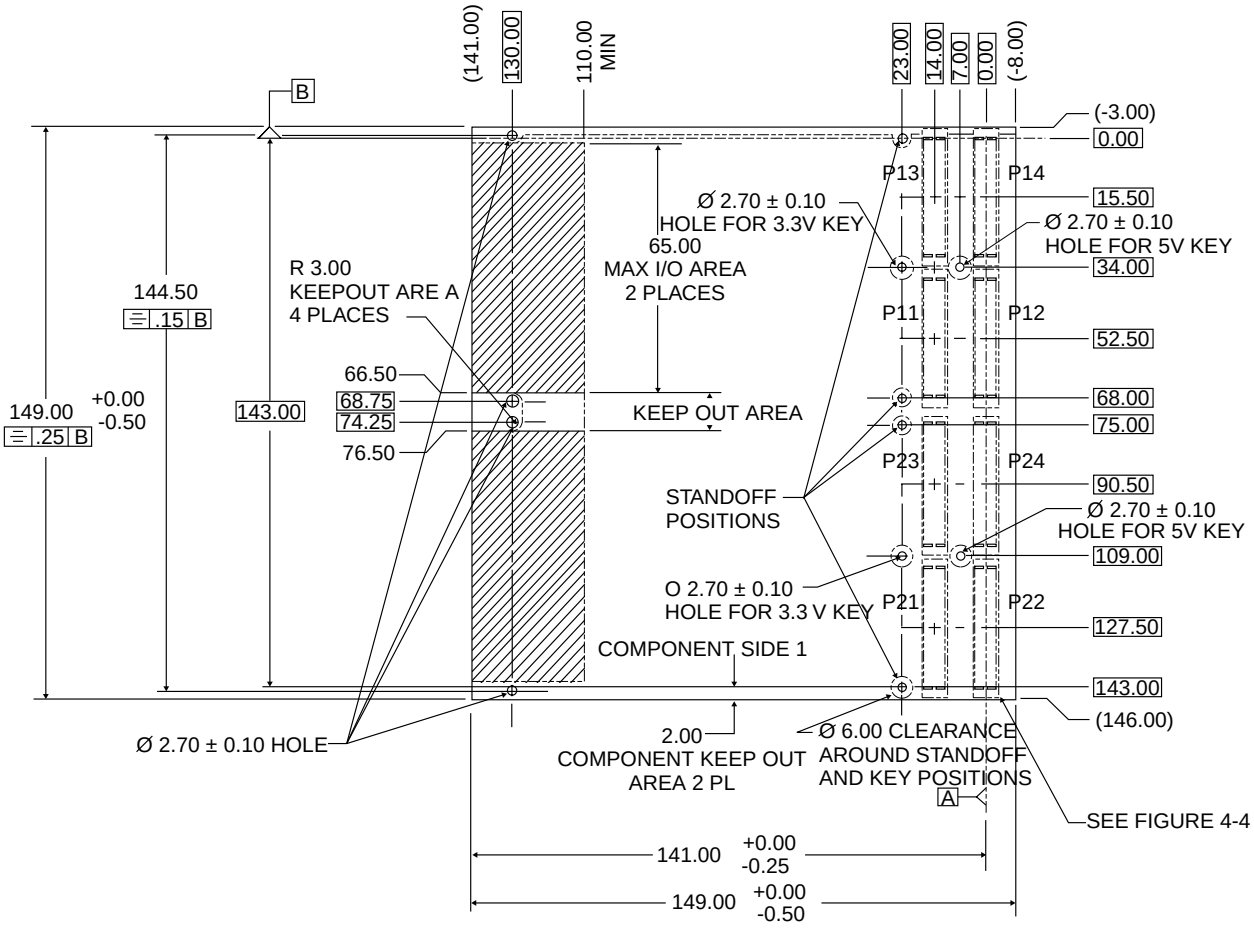

Figure 4-3
Double CMC

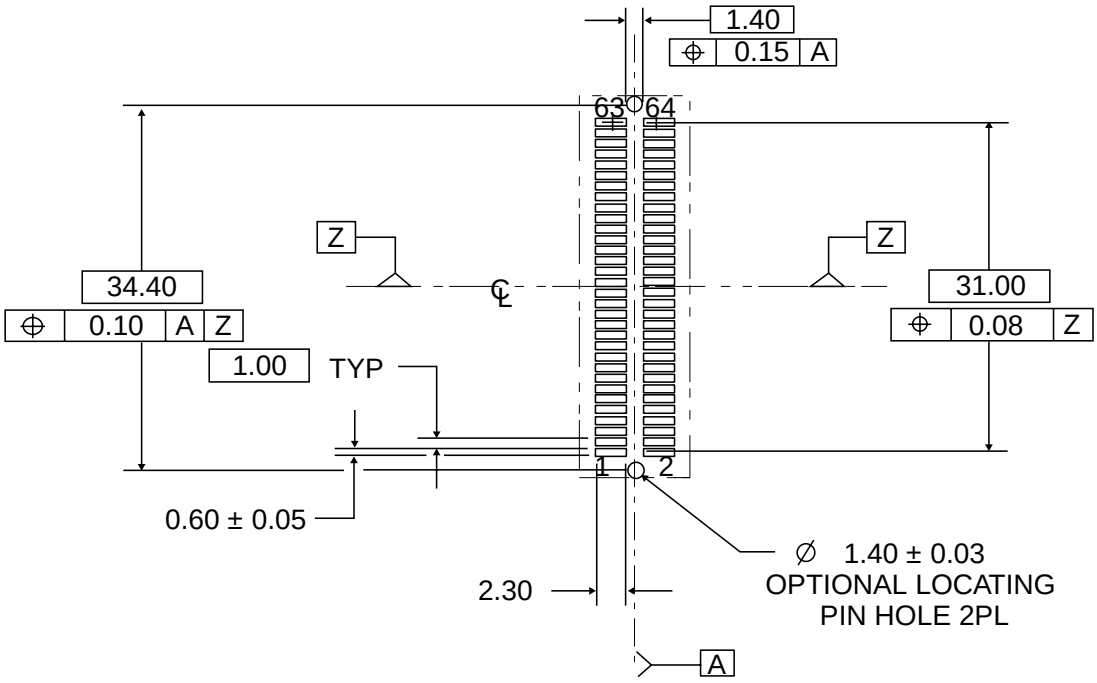

Figure 4-4
CMC "P" Connector Surface Mount Pad

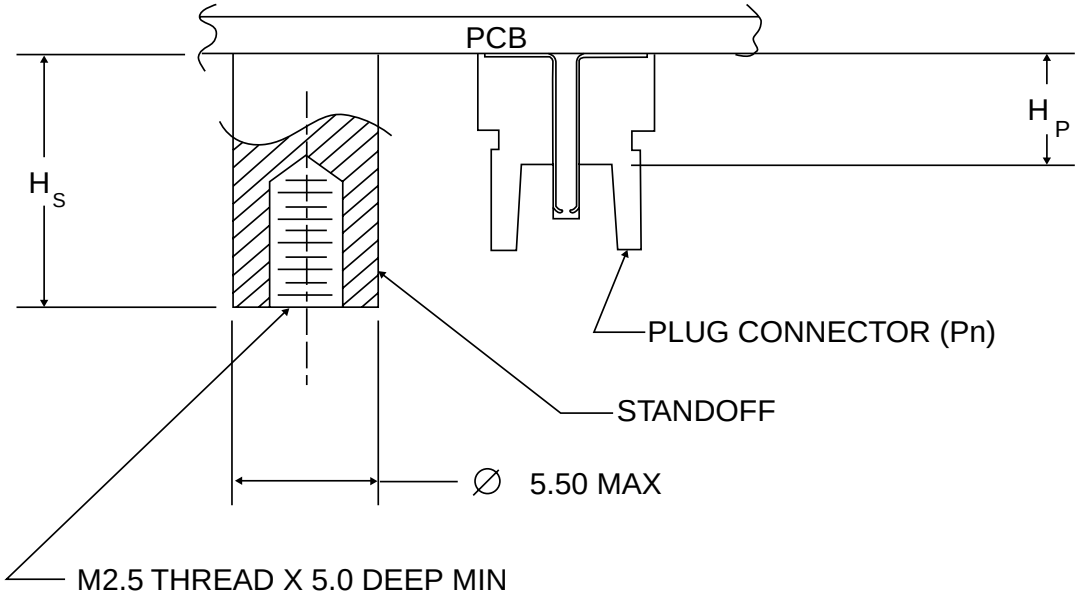

Figure 4-5
CMC Connector and Standoff Relationship

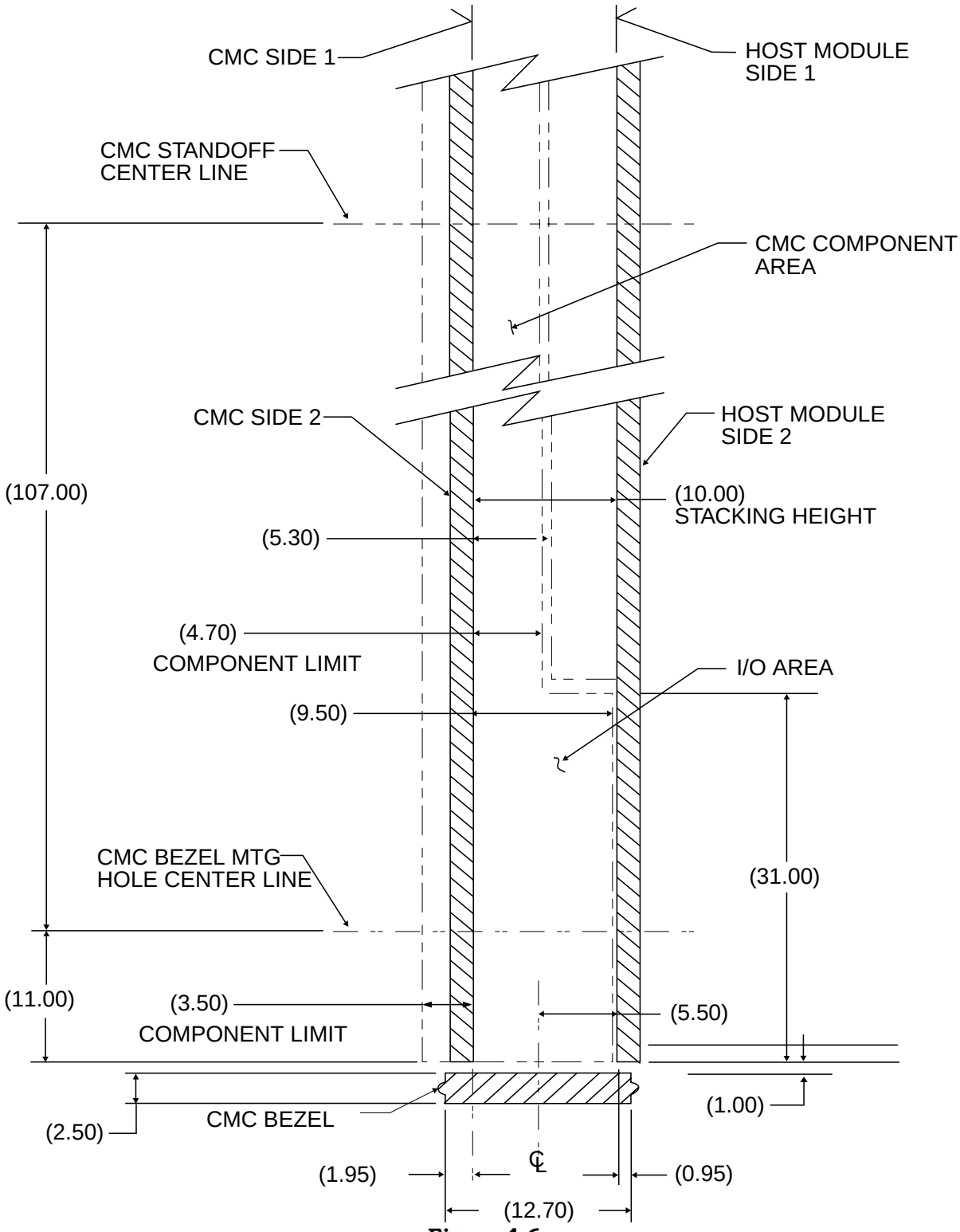

Figure 4-6
CMC I/O Area and Component Area Limits Reference

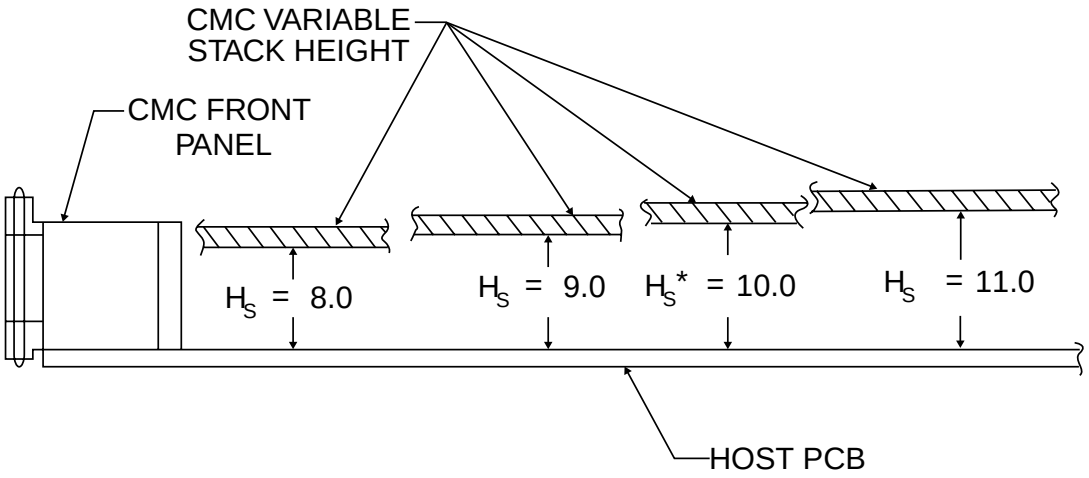

Figure 4-7
CMC PCB Position within Mezzanine Card Envelope

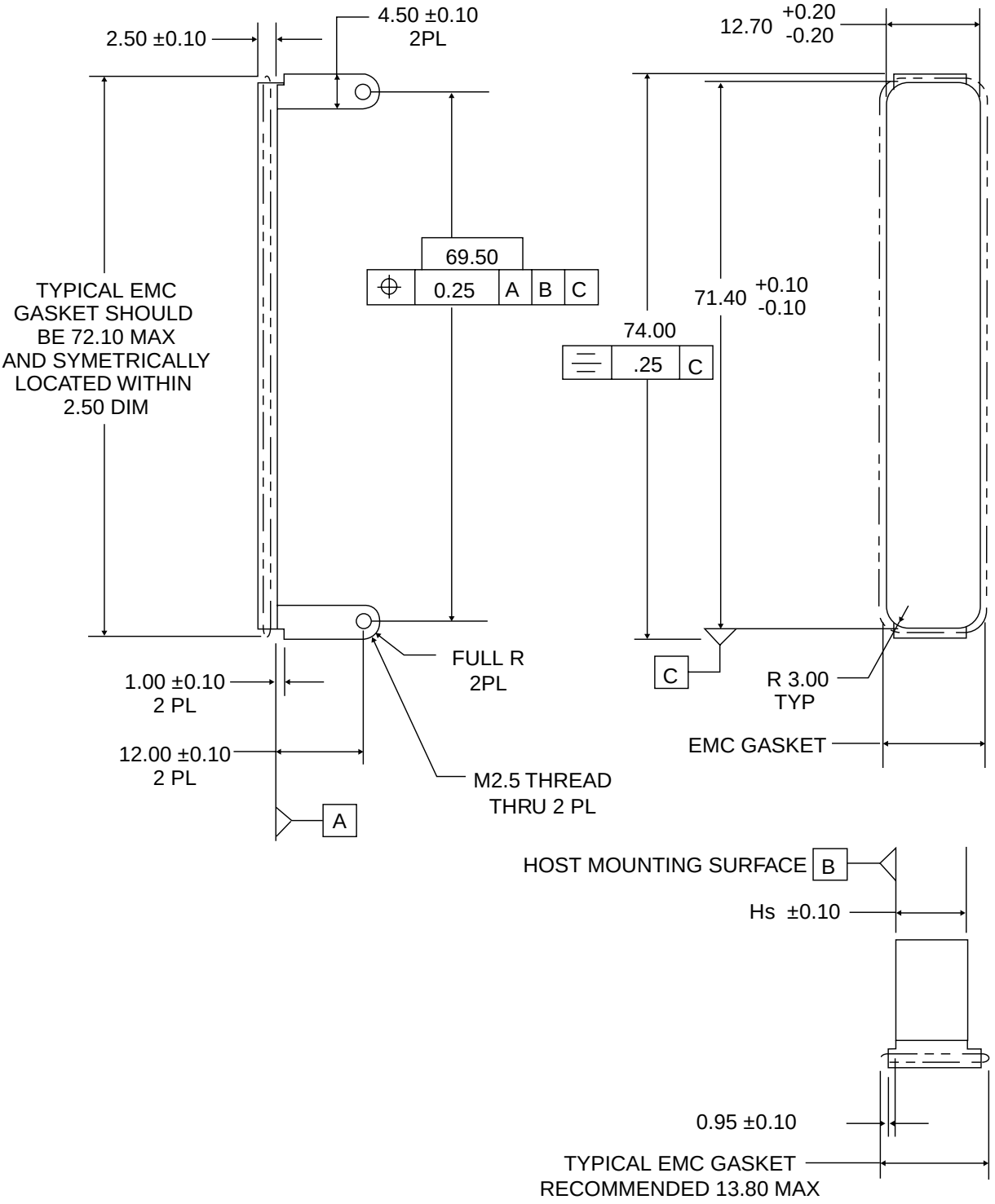

Figure 4-8
CMC Bezel Detail

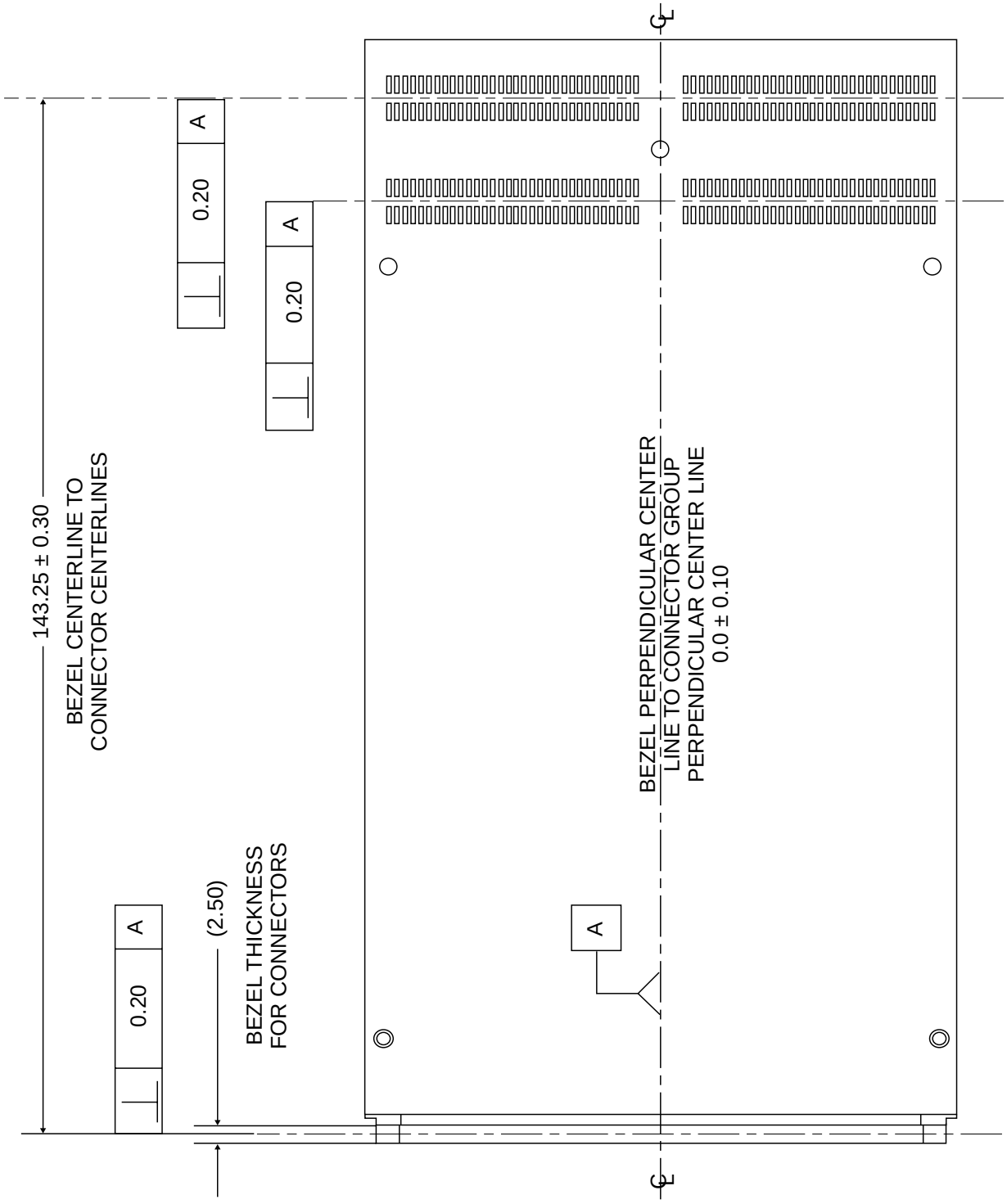

Figure 4-9
Bezel to Connector Test Dimensions

5. Host CMC Slot Mechanics

This chapter defines the mechanical dimensions for the mezzanine card host. The mezzanine card mechanics are defined in chapter 4.

The mechanics for CMC slots on VME64x, CompactPCI, Multibus I, and Multibus II are defined in this chapter. The mechanics for desktop computers, portable computers, servers and other similar types of computers are not defined, since these designs vary from computer to computer and manufacturer to manufacturer. Enough information is presented in this chapter, as well as the previous chapter, for mechanical designers of these types of computers to be able to design hosts with one or more CMC slots.

5.1 Stacking Height Above the Host PCB

The mezzanine card mechanics are designed to be placed within the single slot envelope of VME64x, CompactPCI and Multibus II boards. Usage of these mezzanine cards does not force the host board combined with a mezzanine card to take up two slots. For VME64x, CompactPCI, Multibus I and Multibus II, the referenced stacking height is 10 mm from the host PCB to the mezzanine card PCB. For applications that require more vertical space above the host side 1 surface a 13 mm stacking height is also defined. Taller components can be used underneath the mezzanine card area when 13 mm stacking height is used..

Other stacking heights can be used as well, as long as all the associated connector and shoulders are increased by the same height. Any incremental height changes shall always be in 1 mm steps.

5.2 Host PCB Mechanics

VME64x and CompactPCI host boards can support either one or two CMC slots. The mechanics of these 6U PCBs shall be per Figures 5-1 and 5-2 for one or two slots, respectively. Multibus II host boards can also support one or two CMC slots, which shall be per Figures 5-3 and 5-4, respectively. The Multibus I mechanics shall be per Figures 5-5 and 5-6.

Whenever two slots are provided on the host computer, they shall be adjacent to one another as defined in the respective figures. This will allow for double sized CMCs to be plugged into those slots.

The position of each mezzanine slot, with respect to the front edge of the host computer's PCB is fixed. The vertical position is variable and left open to the designer as to the exact position. The position shown is for reference only and is not a recommendation. This position shall remain within the boundary defined in the referenced figures.

5.2.1 Other Host PCB Mechanics

It is possible to place a single CMC slot on 3U VME64x or CompactPCI boards. It shall fit between both the top and bottom handles. There is no room left for other host front panel switches and indicators.

No drawing is provided for 3U and 9U VME64x or for 3U CompactPCI boards. The design can easily be derived from the 6U mechanical drawings and IEEE 1101.1-1998 Standard, reference

[5]. IEEE 1101.1-1998 defines the mechanics of the 9U form factor. Should boards be designed for the 9U height, up to 4 CMC slots can be provided.

5.3 Connector Pads and Labeling

Figure 5-7 shows the connector pads layout that shall be used for each connector placed on the host PCB. The labeling of each pin within each connector shall also follow the pin numbering scheme shown in Figure 5-7.

Depending on the functionality of the host, anywhere from one to four connectors may be used, and in any combination. Recommendations as to which combinations are used are left to the child standards that use this standard for their mechanical card definition.

5.4 CMC Connectors

All host CMC connectors shall use the EIA E700 AAAB connector as defined by the EIA standard in reference [1]. These connectors shall be referred to as the receptacle, or "Jn" connector. For single slot hosts, the connectors shall be labeled J11 through J14. For two slot hosts, the connector numbers shall be J11 through J14 and J21 through J24. Should three slot hosts be used, the third set of connectors shall be labeled J31 through J34. Note that there are only single and double slot mezzanine cards.

For hosts that support the 10 mm stacking height between the host and the mezzanine card, the 5.3 mm connector shall be used. The 8.3 mm connector height shall be used for hosts that support the 13 mm stacking height. See Figure 5-8 and Table 5-1 for point of reference.

Not all applications will need all the connectors. It is optional as to which combination of connectors are used.

If a host computer does not use all of the connectors, this space is open to be utilized by additional components. A special caution should be noted as a mezzanine card with all connectors mounted could be plugged in to such a host making restricting component heights mandatory. For host computers that do place components, other than connectors in the connector area, these components shall not exceed a height of 1.00 mm for 10.0 mm stacking heights. If 13.0 mm stacking height is used, component height shall not exceed 4.00 mm.

5.5 CMC Connector Assembled on a Host

Assembly of all the CMC connectors on a host PCB shall be within +/- 0.14 mm of true position (TP). TP is defined as some point on a host's PCB, near the connector, that is used by the assembly equipment for positioning of the connector(s) prior to soldering.

The angular mis-alignment of any connector shall not exceed 1.5 degrees, and shall not exceed 0.07 mm of perpendicular mis-placement from one end of the connector to the other end of the connector.

The solder thickness variation between the connector contacts and the solder coated surfaces on the mezzanine card shall not exceed 0.1 mm. Excessive build up of solder under the connector contacts will cause the connector to be mounted too high such that when a mezzanine card is plugged into the host's slot, the plug and receptacle connector seating surface will touch and push against each other with excessive force.

5.6 Host Board Side 1 Component Height

Host designers are allowed to place components under the mezzanine card slot. The maximum height of this area depends on whether the reference plane of the mezzanine card is 10 mm or 13 mm above the host. Table 5-1 lists these heights that shall be used.

Table 5-1
Host Component Height Limits

CMC Reference Place Stacking Height	Receptacle Height Figure 5-8	Components Under CMC Component Area Figure 5-14	Components Under CMC I/0 Area Figure 5-14
10	5.30	4.70	0.00
13	8.30	7.70	2.00

No components shall be placed in the I/O area when the CMC is placed 10 mm above the host. When traces or vias are used in this I/O area, they shall be insulated to prevent shorting, should the mezzanine I/O area touch the host PCB in this area.

When the CMC is placed 13 mm above the host, the host component height under this area shall not exceed 2 mm. The reason for the extra 1 mm of space is for electrical clearance and air flow.

5.7 Extra Shoulder for 13 mm Hosts

For hosts, which support the 13 mm stacking height between the host side 1 and the mezzanine card side 1 reference plane, a 3.0 mm shoulder is needed underneath each of the standoff locations and the bezel legs. See Figure 5-8 for reference. Not shown is the spacer for the CMC bezel.

This shoulder should be attached to the host and must present a clear hole that allows a fastener from the host side to be threaded into the mezzanine standoff. Whenever a shoulder is needed, the shoulder on the host module shall provide a 2.7 mm clearance hole to allow for assembly to the mezzanine card and will have a height that is dependent on the height of the connector receptacle used on the host board.

In event a different stacking height of 10 or 13 mm is used, the shoulder and host receptacle connector heights shall all be increased by the same height. As stated in section 4.1, the incremental height shall be in 1 mm steps.

5.8 Voltage Keying Pins

Many of the new local buses can operate at one of two different voltage levels. Voltage keying pins are required on all host implementations in order to safe guard all installations utilizing the CMC.

The two bus signaling voltages are 5V and 3.3V. If the host's local bus operates on the 5V signaling level, it shall connect 5V to the V(I/O) pins of the connector and provide a 5V keying pin near the connectors. If the host's local bus operates on the 3.3V signaling level, it shall connect 3.3V to the V(I/O) pins of the connector and provide a 3.3V keying pin near the connectors. See Figures 5-1 through 5-6 for location of these keying pin positions and Table 6-1 for the V(I/O) pin assignment.

The mechanics of each voltage keying pin is defined in Figure 5-8. Note that two different length voltage keying pins are defined, one for 10 mm spacing and one for 13 mm spacing. See section 5.1 for other increments.

The associated voltage keying holes for mezzanine cards are defined in the previous chapter.

5.9 Host Front Panel or Host Face Plate Opening

The size and placement of one or two CMC slot openings for VME64x and CompactPCI boards shall be per Figures 5-9 and 5-10 respectively. Multibus II front panel openings mechanics shall be per Figures 5-11 and 5-12.

The horizontal center line of each slot shall be aligned with the center of each CMC connector group. See Figure 5-13.

Note that Multibus I boards do not have front panels. For desktop computers, portable computers, servers and other types of computers with face plates, the mechanics of the CMC slot opening can be derived from the mechanics in Figures 5-9 through 5-12.

5.10 Filler Panels

It is recommended that host computers prepared for shipment without a mezzanine card plugged into a slot should be shipped with an EMC compatible filler panel in the vacant slot opening.

5.11 Host Test Dimensions

It is very important that fully assembled hosts be measured to ensure that when a CMC is plugged into a host's CMC slot, it will comply. Therefore once the host is assembled, there are three critical dimensions that shall be measured to ensure that generic CMCs are in compliance.

The first critical dimension is the depth distance between rear connectors (0.00 reference) and the center line of the host front panel EMC contact area. See Figure 5-13.

The second critical dimension is the horizontal center line dimension, where the center of the front panel opening shall be centered with the CMC connector group. See Figure 5-13.

The third critical dimension is the height of the CMC slot opening's center line above the host's PCB, side 1. This will vary depending on whether a 10 mm or 13 mm spacing is used. See Figure 5-14 for this dimension.

When a CMC is plugged into the host's CMC slot, the CMC's bezel should be aligned with the host computer CMC slot opening. Due to tolerance build up, this will not perfectly match. The actual mismatch may be as much as +/- 0.3 mm.

5.12 I/O Capability

I/O capability may be through the bezel opening or via the backplanes user defined pins (if available). Depending on the host's application, either or both may be used.

For I/O through the host's backplane, such as VME64x, CompactPCI, Multibus I or Multibus II, one or more of the CMC connectors may be assigned for this capability. See chapter 6 of this standard for required signal pin mappings.

5.13 Power Dissipation

The maximum power provided by the host for each mezzanine card slot as well as the heat a host computer must remove from within the host's chassis (box, cabinet, etc.) should be clearly defined. Host computer designers can then design for the worst case in both power draw as well as removal of heat generated by the mezzanine card. See Table 4-3 in the previous chapter for the recommended power consumption and dissipation for each of the mezzanine card sizes.

Since the mezzanine card side 1 faces the host side 1, the power dissipated underneath the mezzanine card should be limited to prevent excessive heat build up in the area between the two. See Table 5-2 for the recommended maximum heat dissipation levels on side 1 of the host of the area where CMC is placed.

Table 5-2
Host Side 1 Maximum Heat Dissipation

Stacking Height (mm)	Max Watts
10.0	4.0
13.0	6.0

5.14 Grounding Connections

Mezzanine cards shall be designed to minimize potential ground loop and EMC problems. CMC bezels shall be electrically isolated from the mezzanine card's signal ground plane and shall meet the minimum requirements in section 4.14. For CMC's with I/O cables exiting the system chassis, the CMC's bezel should be attached to the host board chassis ground. For CMC's with no I/O cables exiting the system chassis, the CMC bezel may be grounded to the host board chassis ground or be left floating as required by the application. All mezzanine card standoffs (those standoffs near P11 and P13) should be tied to circuit ground at both the mezzanine card and the host board to avoid any "antenna" effects and to minimize the ground difference between the host and mezzanine card. [Early drafts of this standard, did not recommend connecting the mezzanine circuit ground to host circuit ground via the standoffs, but later design experience recommends the opposite.]

All keying pins shall be tied to the host's circuit ground, since the keying hole in the mezzanine card is to be electrically isolated from the rest of the mezzanine card's circuits.

5.15 Electromagnetic Compatibility

The Electromagnetic Compatibility (EMC) for host computers is not specified in this standard. It is recommended that host computer vendors clearly specify to what EMC standards and to which levels the computer has been designed and tested to. Host designers should study the mezzanine card requirements in the previous chapter to understand what each mezzanine card is required to support, and then determine what is the most appropriate design for the host computer.

5.16 Environmental

The temperature, humidity and other climatic environmental requirements are not specified in this standard, since these requirements are application dependent. It is recommended that host computer vendors clearly specify to what environmental level the computer can operate and to which national and international environmental standards the computer was designed and tested.

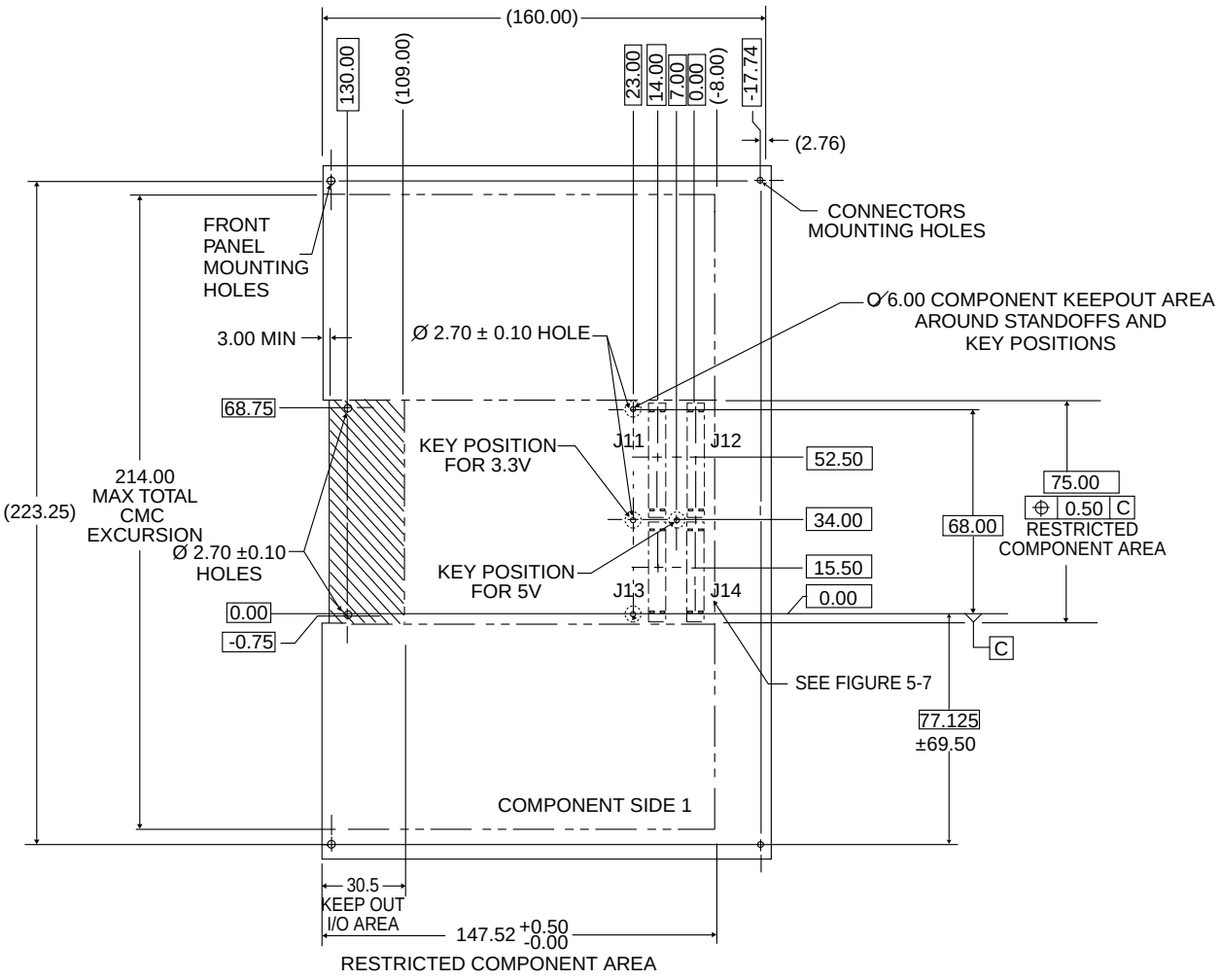

Figure 5-1
VME64x or CompactPCI Host for Single CMC

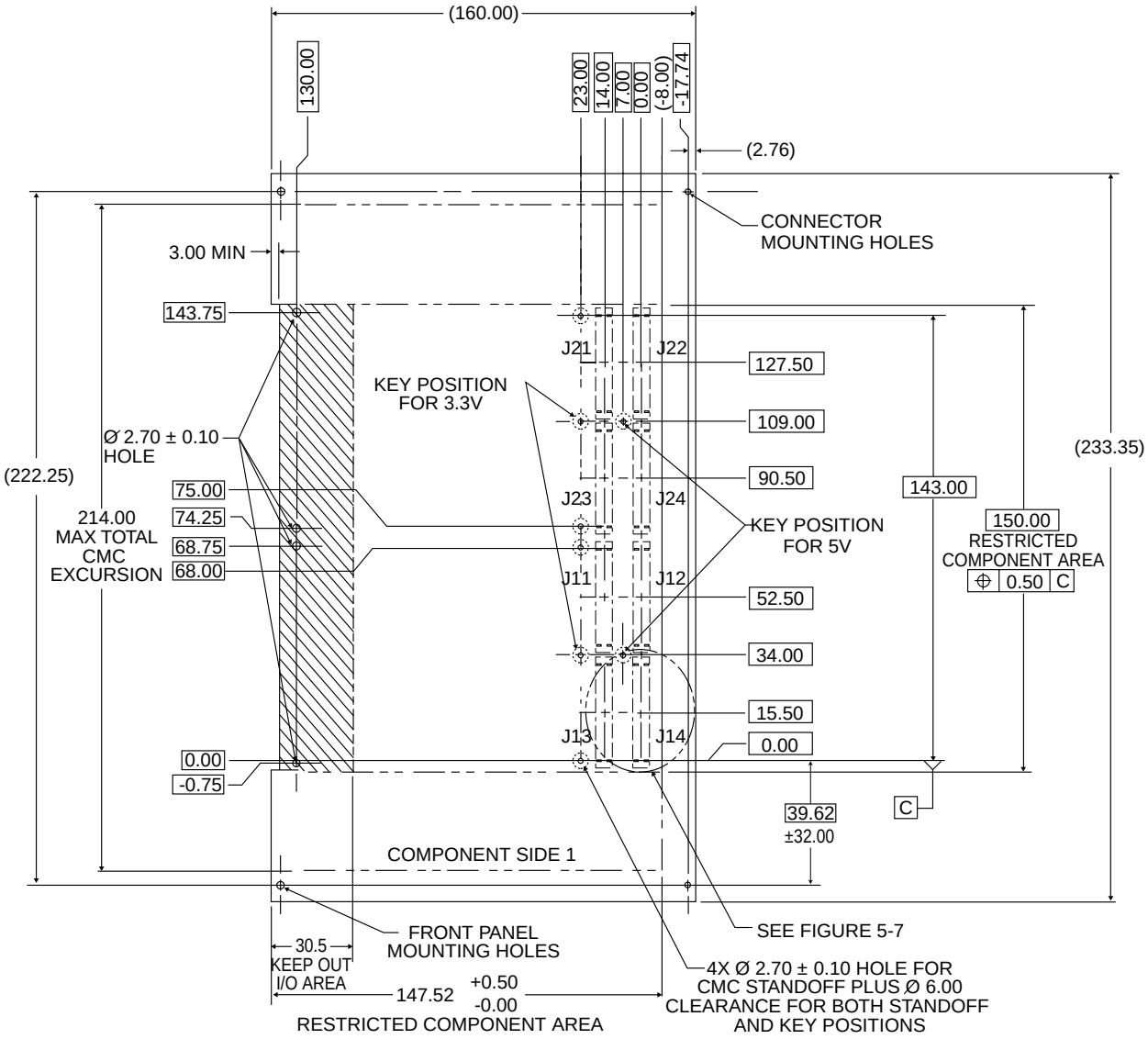

Figure 5-2
VME64x or CompactPCI Host for Double or Two Single CMCs

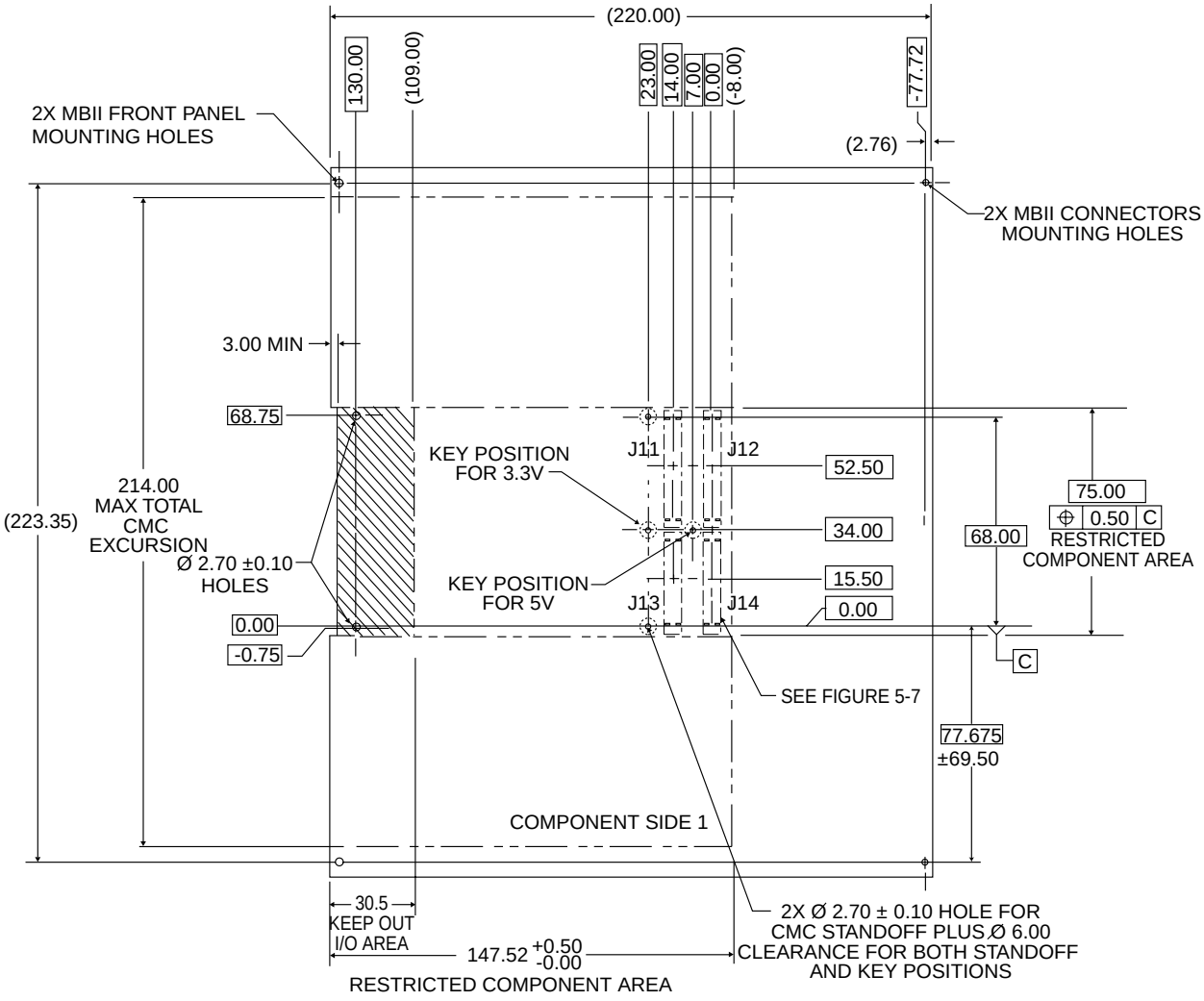

Figure 5-3
Multibus II Host for Single CMC

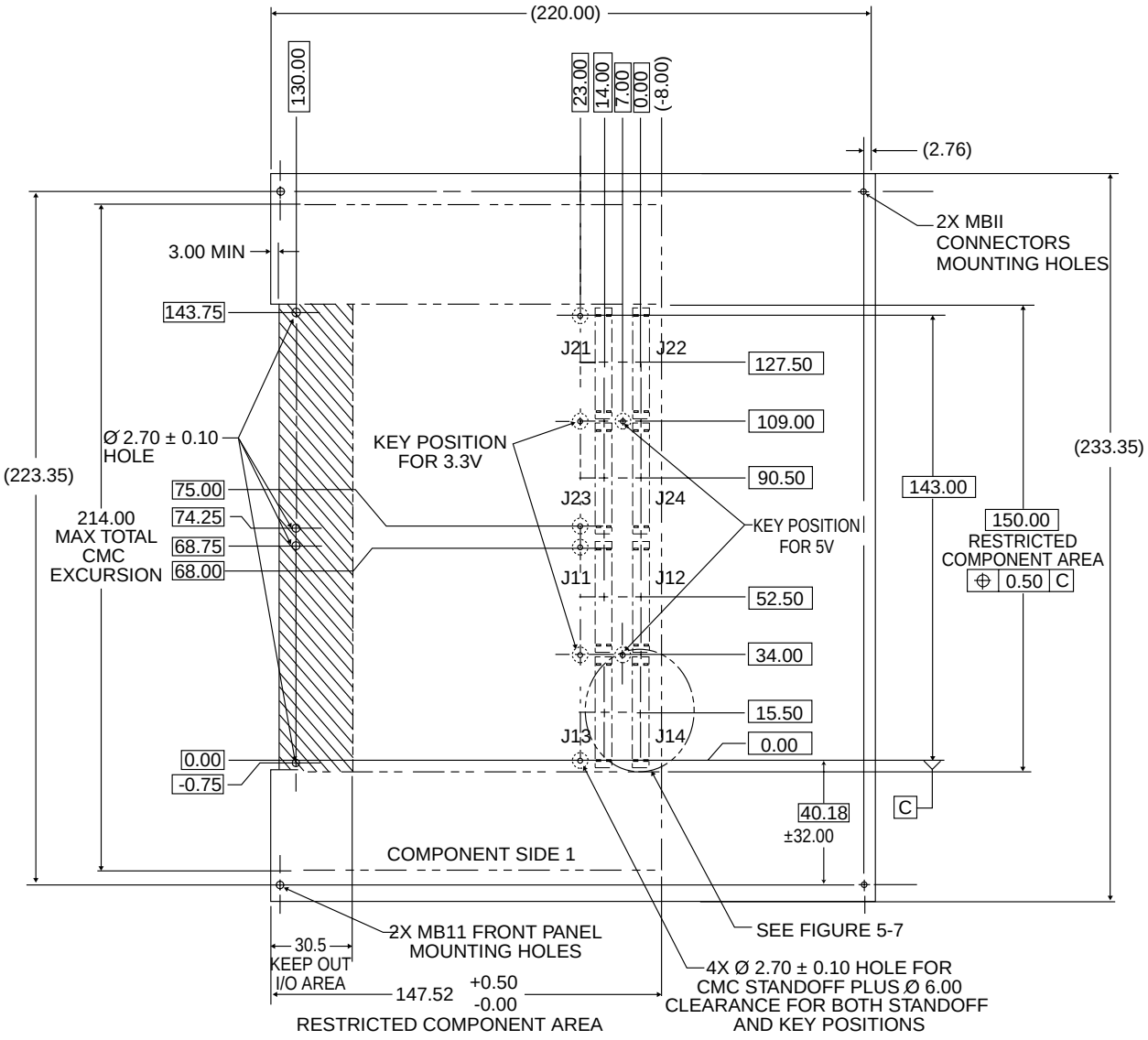

Figure 5-4
Multibus II Host for Double or Two Single CMCs

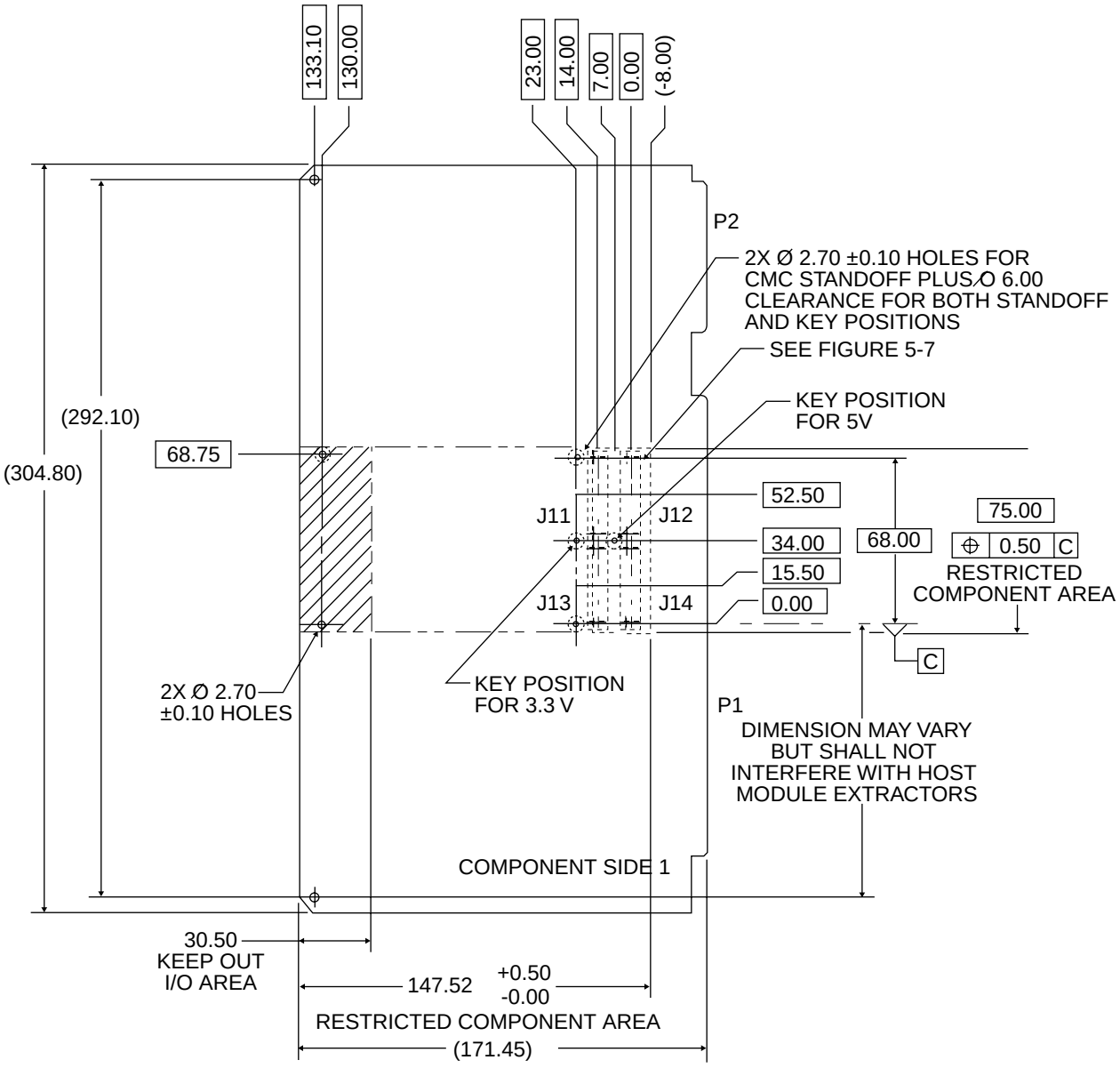

Figure 5-5
Multibus I Host For Single CMC

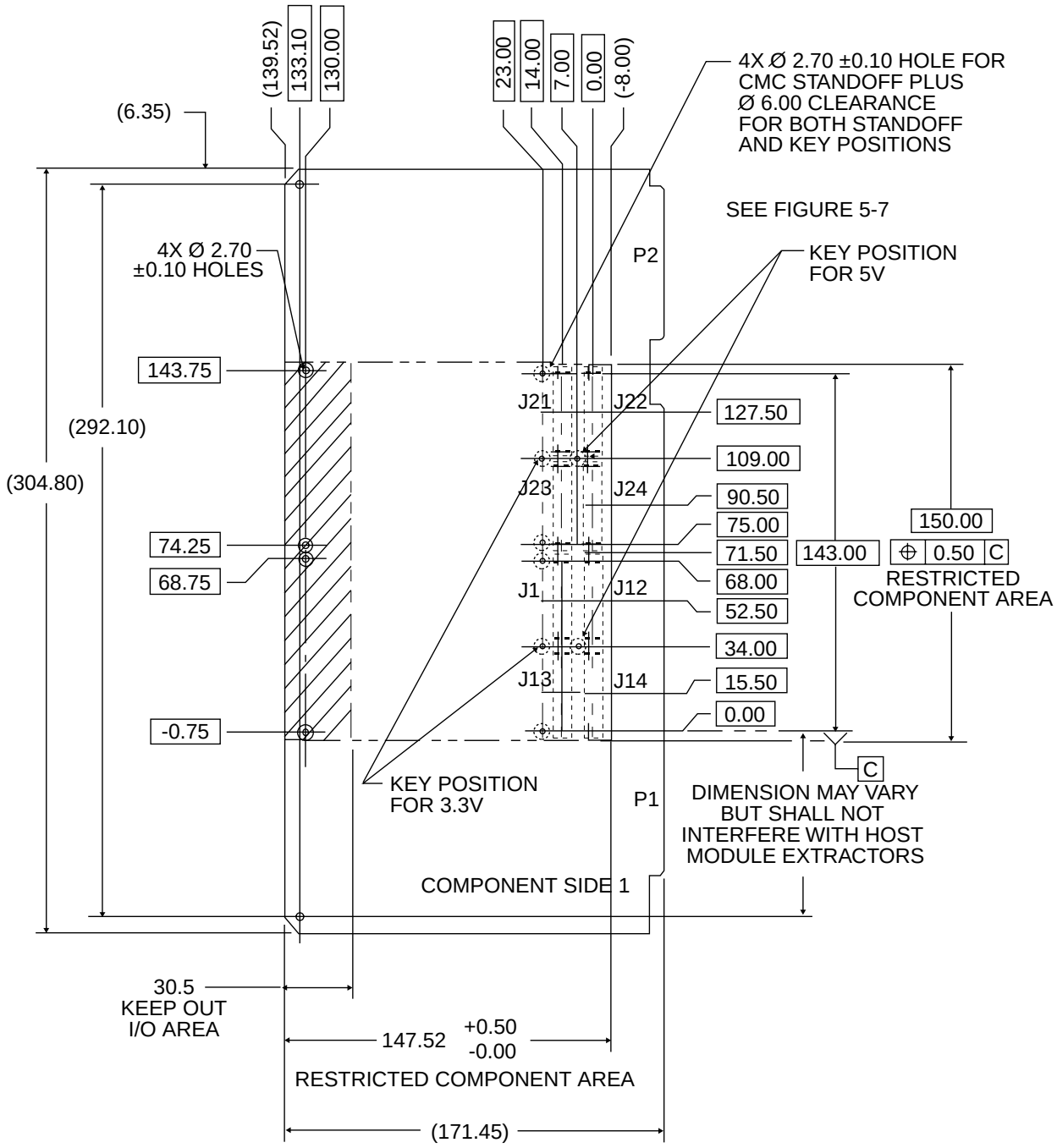

Figure 5-6
Multibus I Host for Double or Two Single CMCs

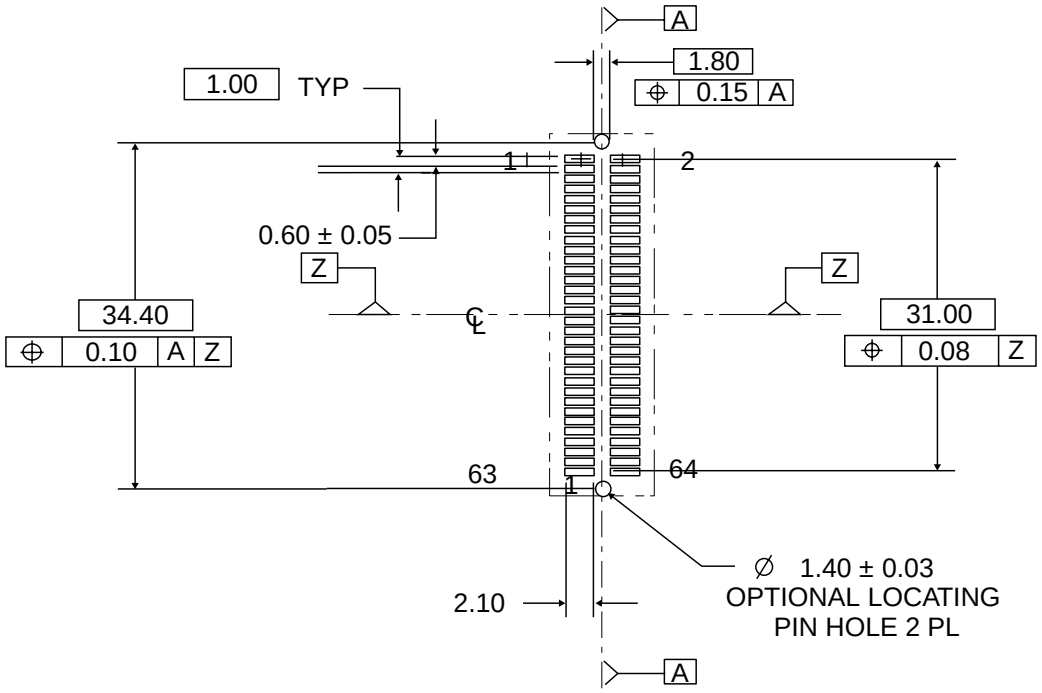

Figure 5-7
Host "J" Connector Surface Mount Pad Layout

Note: (1) is for 10.0 mm stacking height
(2) is for 13.0 mm stacking height

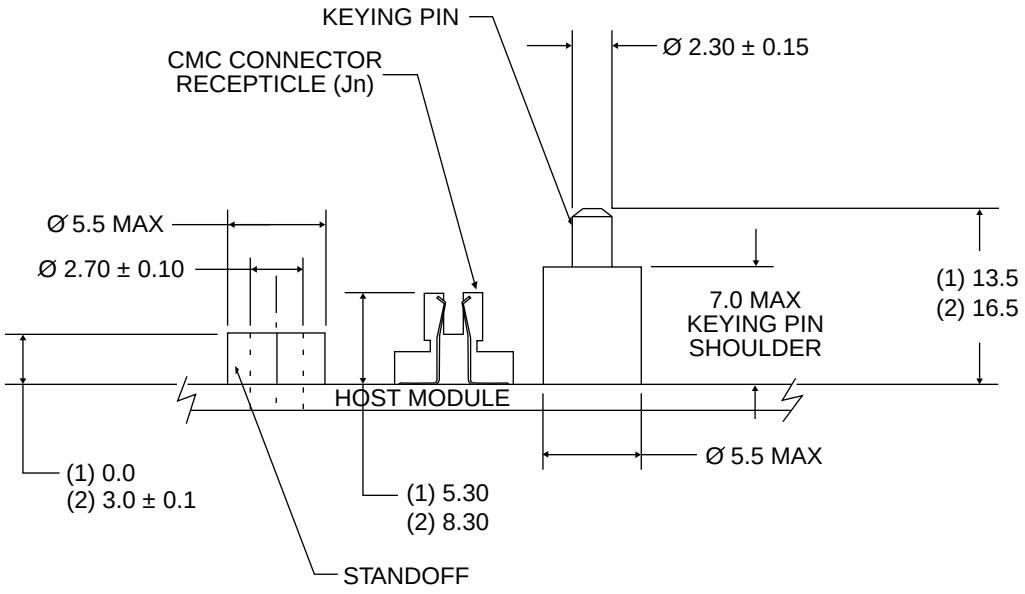

Figure 5-8
Host Side View of Standoff, Receptacle and Keying Pin

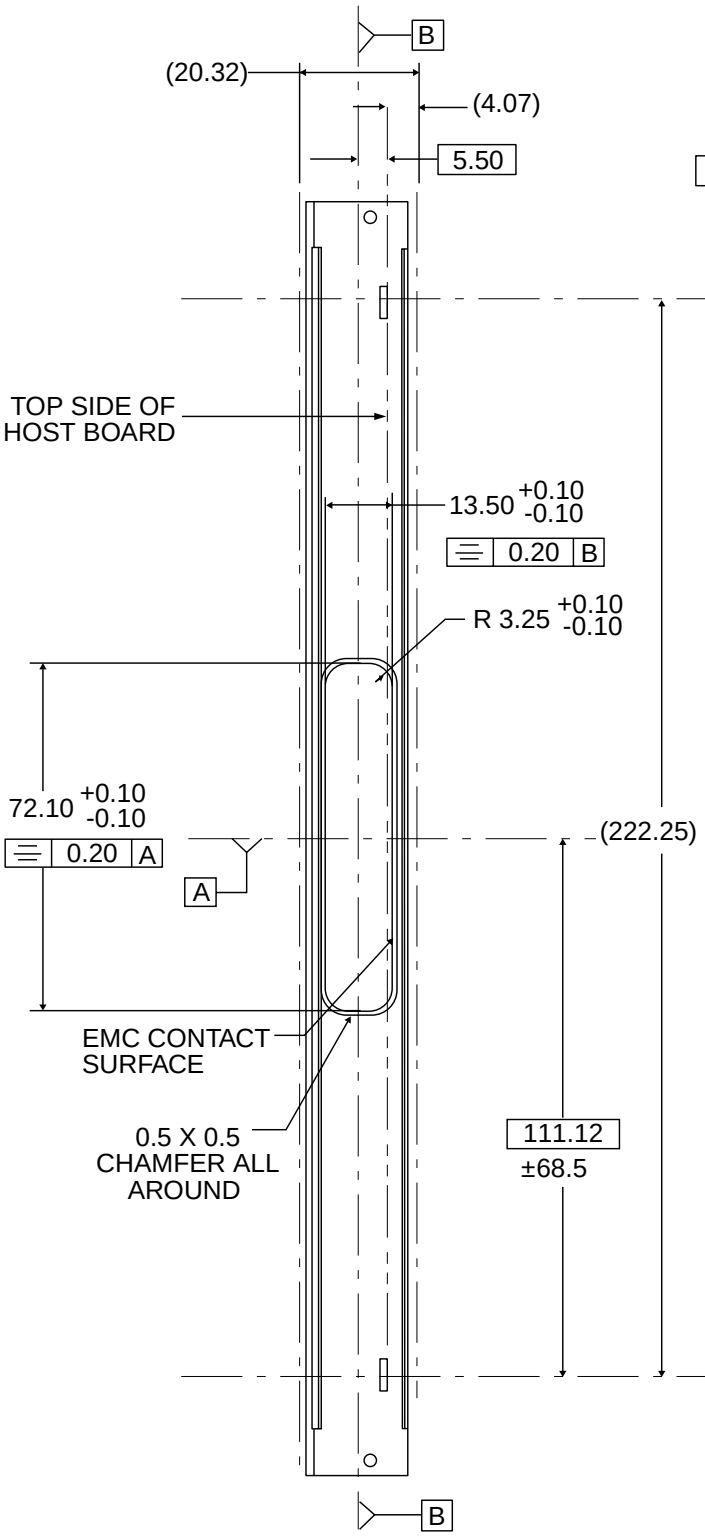

Figure 5-9
VME64x or CompactPCI Front Panel with Single Slot CMC, Rear View

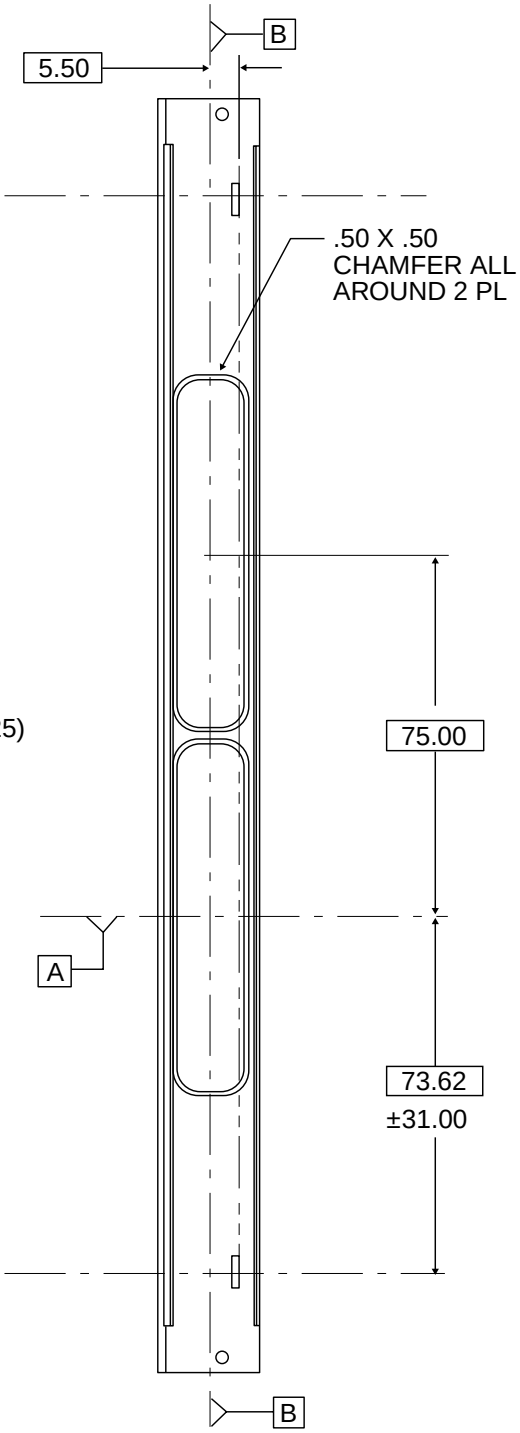

Figure 5-10
VME64x or CompactPCI Front Panel with Double Slot CMC, Rear View

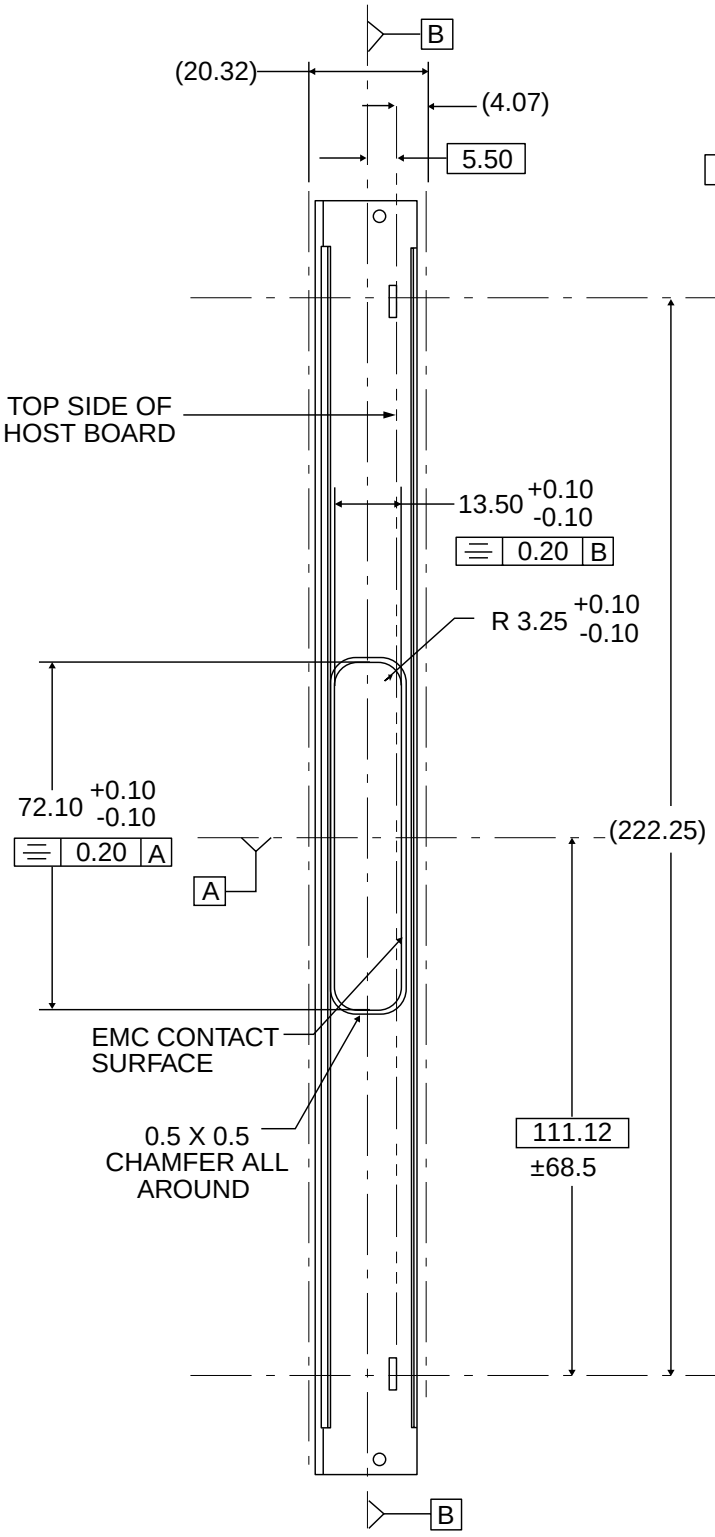

Figure 5-11
Multibus II Front Panel with CMC Slot, Rear View

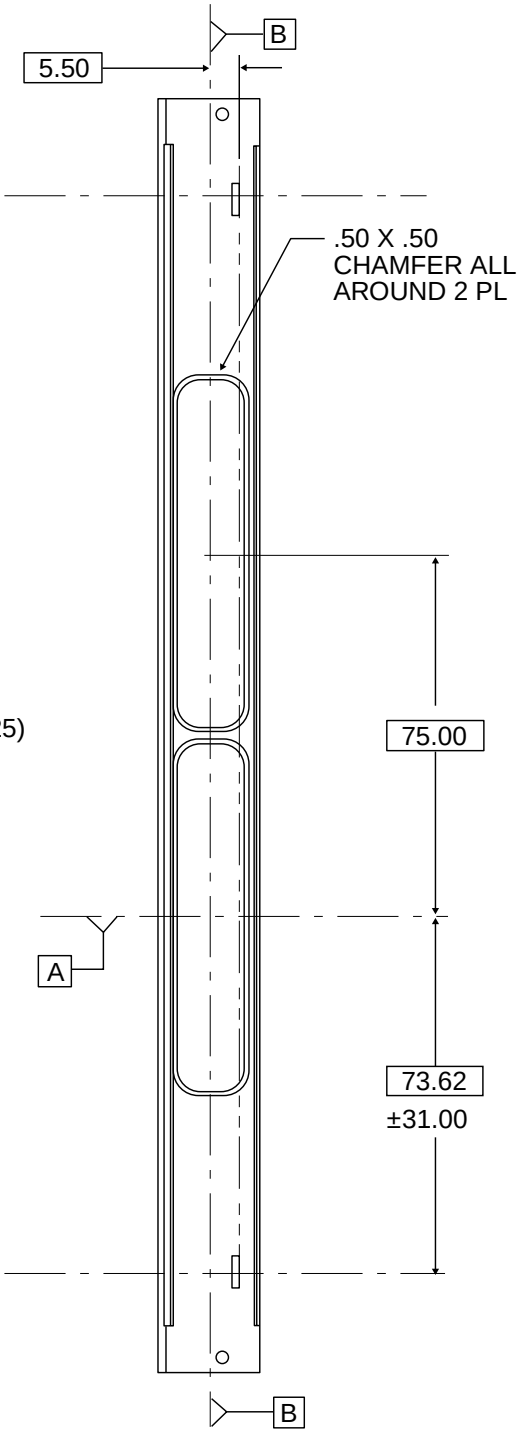

Figure 5-12
Multibus II Front Panel with Two CMC Slots Rear View

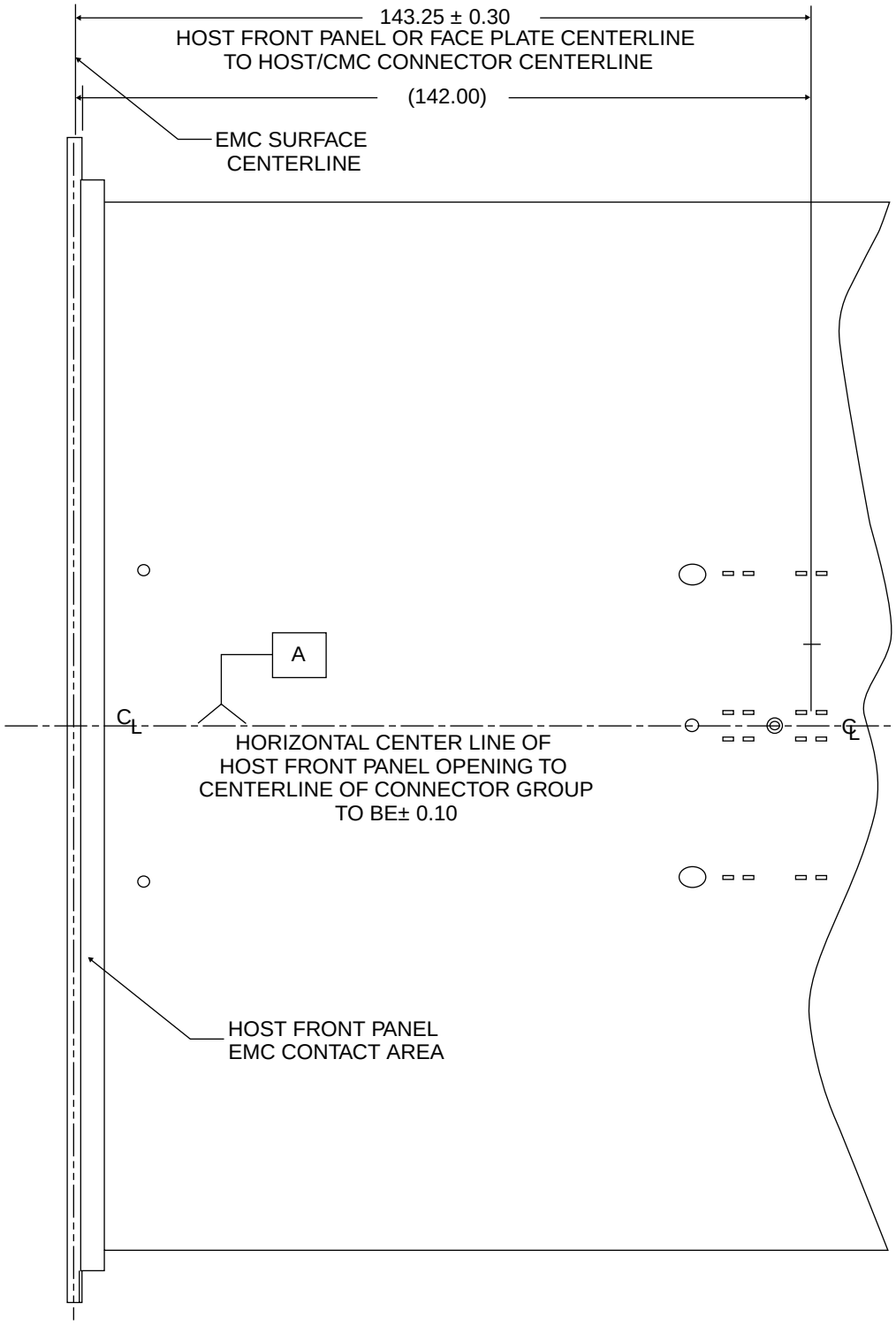

Figure 5-13
EMC Host Contact Area

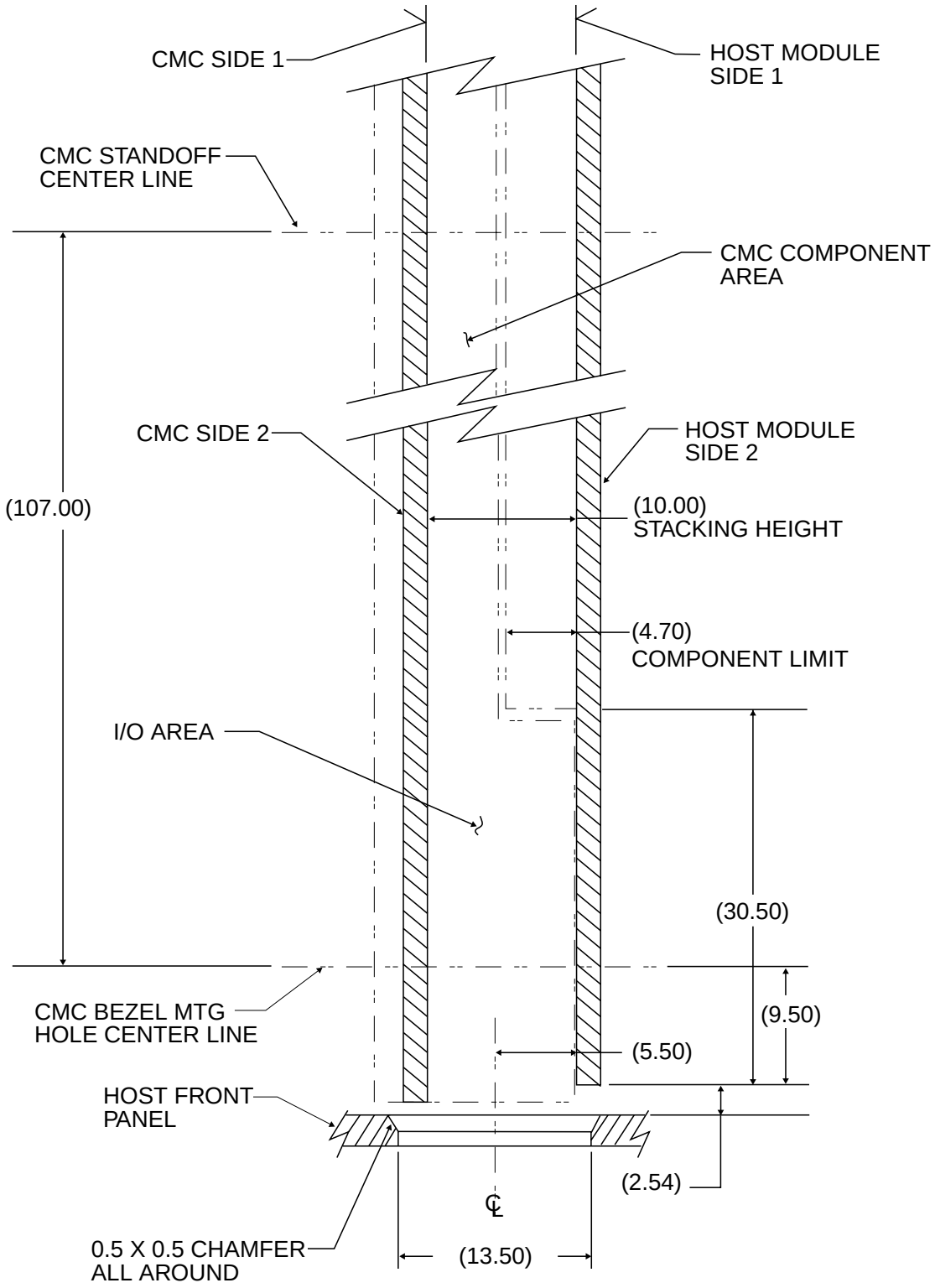

Figure 5-14
Host Component Limits Reference
(For IEEE 1101.1 compatible Printed Circuit Boards)

6. Electrical and Logical Layers

6.1 Connector Utilization

The CMC connector pin assignments are based on specific signal integrity rules as well as power considerations. The CMC standard allows +5V, +3.3V and +/- 12V. Which of these voltages shall be provided is defined in the specific bus standard: however, if used, the voltages shall be provided on the pins specified. The + 5V pins are assigned to Pn1 connector, the + 3.3 volt pins are assigned to the Pn2 connector and the V(I/O) (signaling voltage) to Pn1 and Pn3 connector. All signal pins are surrounded by either voltage or ground pins. Pn1-13 is surrounded by three ground pins and is recommended for critical signals such as the clock signal.

The Pn4 connector is for user defined functions such as I/O. Routing of I/O traces on the host shall follow the I/O mapping as specified in Section 6.3.3.

6.2 CMC Connector Pin Assignments

The following table provides all common pin assignments and signal names for the CMC application.

Table 6-1
CMC Connectors Pin Assignments

Pn1/Jn1				Pn2/Jn2			
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Pin #**	**Singal Name**	**Signal Name**	**Pin #**
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V(I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Gnd or Signal	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

Table 6-1 (Continued)
CMC Connectors Pin Assignments

Pn3/Jn3				Pn4/Jn4			
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Pin #**	**Singal Name**	**Signal Name**	**Pin #**
1	Signal	Ground	2	1	I/O	I/O	2
3	Ground	Signal	4	3	I/O	I/O	4
5	Signal	Signal	6	5	I/O	I/O	6
7	Signal	Ground	8	7	I/O	I/O	8
9	V(I/O)	Signal	10	9	I/O	I/O	10
11	Signal	Signal	12	11	I/O	I/O	12
13	Signal	Ground	14	13	I/O	I/O	14
15	Ground	Signal	16	15	I/O	I/O	16
17	Signal	Signal	18	17	I/O	I/O	18
19	Signal	Ground	20	19	I/O	I/O	20
21	V(I/O)	Signal	22	21	I/O	I/O	22
23	Signal	Signal	24	23	I/O	I/O	24
25	Signal	Ground	26	25	I/O	I/O	26
27	Ground	Signal	28	27	I/O	I/O	28
29	Signal	Signal	30	29	I/O	I/O	30
31	Signal	Ground	32	31	I/O	I/O	32
33	Ground	Signal	34	33	I/O	I/O	34
35	Signal	Signal	36	35	I/O	I/O	36
37	Signal	Ground	38	37	I/O	I/O	38
39	V(I/O)	Signal	40	39	I/O	I/O	40
41	Signal	Signal	42	41	I/O	I/O	42
43	Signal	Ground	44	43	I/O	I/O	44
45	Ground	Signal	46	45	I/O	I/O	46
47	Signal	Signal	48	47	I/O	I/O	48
49	Signal	Ground	50	49	I/O	I/O	50
51	Ground	Signal	52	51	I/O	I/O	52
53	Signal	Signal	54	53	I/O	I/O	54
55	Signal	Ground	56	55	I/O	I/O	56
57	V(I/O)	Signal	58	57	I/O	I/O	58
59	Signal	Signal	60	59	I/O	I/O	60
61	Signal	Ground	62	61	I/O	I/O	62
63	Ground	Signal	64	63	I/O	I/O	64

6.3 Rear I/O Mapping

This section defines the recommended mapping of the CMC's Jn4 I/O connector to the rear I/O connectors on VME64, VME64x, Multibus I and Multibus II boards. These rear I/O connectors attached to the respective backplanes, thereby providing I/O on the rear side of the backplane.

All the tables in this section are organized in the same top view (component side) physical connector pin hole orientation as the rear I/O connectors are attached to the respective printed circuit board. Entries in each table are of the CMC's Jn4 connector pin number. See Figure 5-7 for the CMC Jn4 connectors physical orientation and pin numbering sequence. All I/O signal mappings are done with none to a minimum of crossovers.

6.3.1 I/O Mapping for VME, VME64 and VME64x Boards

I/O Mapping for VME, VME64 and VME64x 3U and 6U boards is controlled and specified by VITA (VME International Trade Association). These I/O mappings can best be found by investigating the following web site: www.vita.com.

6.3.2 I/O Mappings for CompactPCI Boards

I/O Mapping for CompactPCI 3U and 6U boards is controlled and specified by PICMG (PCI Industrial Computers Manufacturers Group). These I/O mappings can best be found by investigating the following web site: www.picmg.com.

6.3.3 I/O Mapping for Multibus II Boards

Multibus II boards provides the whole P2 connector, 96 pins (rows a, b & c) for user defined I/O. For CMC type applications, only connector rows a & c are used for CMC I/O.

Two different I/O mapping schemes are defined for Multibus II host boards: one CMC slot and two CMC slots.

1. For one CMC slot is provided on Multibus II host boards, all 64 pins of the CMC's J14 connector may be mapped to the P2 connector as shown in Table 6-2.

2. When two CMC slots are provided on VME64 and Multibus II host boards, half of each CMC's Jn4 connector's I/O signal lines may be mapped to the P2 connector as shown in Table 6-3.

Note that a two CMC slot host has the option of only mapping one of its' CMC Jn4 connector pins to the P2 connector and leaving the second CMC Jn4 connector un-mapped. In this configuration, it is recommended that lower CMC slot's be mapped to the P2 connector and the upper CMC slot's be un-mapped.

Table 6-2
One CMC Slot's Jn4 Connector Mapped to the Multibus II P2 Connector

P2 Pin Position	P2 Row c	P2 Row a
1	1	2
2	3	4
3	5	6
4	7	8
5	9	10
6	11	12
7	13	14
8	15	16
9	17	18
10	19	20
11	21	22
12	23	24
13	25	26
14	27	28
15	29	30
16	31	32
17	33	34
18	35	36
19	37	38
20	39	40
21	41	42
22	43	44
23	45	46
24	47	48
25	49	50
26	51	52
27	53	54
28	55	56
29	57	58
30	59	60
31	61	62
32	63	64

Table 6-3
Two CMC Slot's J14 and J24 Connectors Mapped to the Multibus II P2 Connector

P2 Pin Position	Row c	Row a
1	J24-1	J24-2
2	J24-3	J24-4
3	J24-5	J24-6
4	J24-7	J24-8
5	J24-9	J24-10
6	J24-11	J24-12
7	J24-13	J24-14
8	J24-15	J24-16
9	J24-17	J24-18
10	J24-19	J24-20
11	J24-21	J24-22
12	J24-23	J24-24
13	J24-25	J24-26
14	J24-27	J24-28
15	J24-29	J24-30
16	J24-31	J24-32
17	J14-1	J14-2
18	J14-3	J14-4
19	J14-5	J14-6
20	J14-7	J14-8
21	J14-9	J14-10
22	J14-11	J14-12
23	J14-13	J14-14
24	J14-15	J14-16
25	J14-17	J14-18
26	J14-19	J14-20
27	J14-21	J14-22
28	J14-23	J14-24
29	J14-25	J14-26
30	J14-27	J14-28
31	J14-29	J14-30
32	J14-31	J14-32

6.3.4 I/O Mapping for Multibus I Boards

There are 40 nonbussed pins available on the Multibus I P2 auxiliary connector. For a Multibus I using one CMC position mapped to P2, 32 backplane I/Os shall be mapped to the P14 connector of the CMC position using the pattern shown in Table 6-4. The second CMC position is not mapped due to limited pins available on P2.

Note: When CMC cards use 32 or less I/O leads, these I/Os shall be assigned to the lower 32 pins.

Table 6-4
One CMC slot on Mulitbus I

Host J14	Multibus I P2	Host J14	Mutibus I P2
33	32	49	16
34	31	50	15
35	30	51	14
36	29	52	13
37	28	53	12
38	27	54	11
39	26	55	10
40	25	56	9
41	24	57	8
42	23	58	7
43	22	59	6
44	21	60	5
45	20	61	4
46	19	62	3
47	18	63	2
48	17	64	1

6.4 BUSMODE Signals

The use of the 4 BUSMODE signals allows: 1) The detection of a CMC card plugged into the host module. 2) To determine the logical protocol the CMC card is capable of handling. 3) To select a common logical protocol for all CMC cards and Host to use.

The 4 BUSMODE signals used by each CMC card are broken up into 2 groups. The first group is a set of 3 signals (BUSMODE[4:2]#) which are bussed to all card slots and the host logic. The second group is a separate return signal (BUSMODE1#), from each CMC card slot to the host logic. The BUSMODE[4:2]# signals are driven by the Host module to all CMC slots, where they are used to determine the mode of the bus to be used by the CMC cards. Each CMC card will receive these signals and use the information to both set the logical protocol it uses on the bus and indicate back to the host module its presence if it can support that logical protocol. The BUSMODE1# signal is driven independently by each CMC card to indicate to the host both the presence of a card in that slot and the capability of performing a given logical protocol. The Host module then uses a read register to sense all the BUSMODE1# signals from each of the CMC slots to determine the presence of CMC cards.

Note that a low logic level "L" has a voltage that is lower (less than) than the high logic level "H".

6.4.1 BUSMODE[4:2]# Signals

The BUSMODE[4:2]# signals are used to determine the presence of cards plugged into the Host module and to set the logical protocol of the CMC bus. These signals are bussed across all the CMC slots and are driven by the Host module logic. The Host module logic is the only logic that shall drive these signals. All CMC slots shall receive these signals as input only signals. The logic levels used by these signals shall be the same as that used by the other bussed CMC signals. The logic level of these signals is determined by the V(I/O) pins and keying on the CMC card. Table 6-5 indicates the encoding of the various bus modules on the BUSMODE[4:2]# signals. The values in the table are taken relative to the signal levels presented on the bussed signals.

Table 6-5
BUSMODE[4:2]# Mode Encoding

BUSMODE4#	BUSMODE3#	BUSMODE2#	Mode
L	L	L	Card Present Test: "Card Present" only if a card is plugged into the slot, no bus protocol should be used
L	L	H	Return "Card Present if PCI capable and uses PCI protocol
L	H	L	Reserved
L	H	H	Reserved
H	L	L	Reserved
H	L	H	Reserved
H	H	L	Reserved
H	H	H	No host present

The BUSMODE[4:2]# signals allows the host module to:

1) Detect if a card is plugged into each of the slots by using the "0" mode where CMC assert the BUSMODE1# signal if they are plugged in regardless of the protocols they support.

2) Sense which protocols each of the cards can handle by using the defined modes ("1" at this time), since a card shall assert a BUSMODE1# signal only if it is capable of that mode.

3) Select which mode the bus shall operate in. Once the host has determined which modes the CMC cards can support, it sets the mode of operation to that which all the cards are capable of supporting. If the host module is incapable of supporting any of the modules, it can then report this as an unsupported bus system.

6.4.2 BUSMODE1# Signal

The BUSMODE1# signal is used by the CMC to indicate its presence in the system. One BUSMODE1# signal is used per CMC connector set. A CMC shall drive the BUSMODE1# signal and the Host module shall only receive the signal. The logic levels used by this signal shall be the same as that used by the other bussed CMC signals, as determined by the V(I/O) pins and keying on the CMC cards. The BUSMODE1# signal shall be asserted by the CMC card within 10 bus clock cycles in response to the mode driven on the BUSMODE[4:2]# signals by the Host module per Table 6-6 below. If a selected mode is not supported by a CMC card then it shall disconnect itself from the bus, i.e. not drive any bus signals, and deassert the BUSMODE1# signal.

Table 6-6
CMC Presents to System

BUSMODE[4:2]#	CMC Capabilities	BUSMODE1#
L L L	Independent of CMC	L
L L H	Capable of performing PCI protocol	L
L L H	Incapable of performing PCI Protocol	H
L H L	Capable of performing “Reserved” Protocol	L
L H L	Incapable of performing “Reserved Protocol	H
LHH -> HHL	Independent of CMC	H
H H H	Independent of CMC	H

As can be seen from the table the BUSMODE1# signal allows the CMC card to:

1) Indicate its presence in the system through the assertion of BUSMODE1# ("CardPresent Mode").

2) Indicate its ability to perform a given logical protocol.

6.4.3 Host Module Logic

The host module needs a 3 bit programmable register to drive the BUSMODE[4:2]# signals and a one-bit read only register to sense the BUSMODE1# signals from each CMC slot. The register used by the Host module to drive BUSMODE[4:2]# should be a read/write register so the system has the ability to read the current mode of the bus. The register used to sense the BUSMODE1# signals from each slot should be synchronized to the system clock. Software/Firmware on the Host module shall insure that an adequate period of time lapses between changing the BUSMODE[4:2]# signals and reading the BUSMODE1# signals. This minimum time period shall be 10 bus clock cycles long. If the Host module is only capable of a single logical protocol then it may "hardwire" or drive that BUSMODE[4:2]# encoding all the time.

6.4.4 CMC Card Logic

The CMC card logic receives the state of the BUSMODE[4:2]# signals and then using knowledge of its capabilities drives its BUSMODE1# signal. This logic should be combinatorial in nature as there is a minimum time of 10 bus clock cycles in which to respond to a change in the BUSMODE[4:2]#signals. This logic also needs knowledge about the capabilities of the CMC card. This can either be programmed into the logic, selected by various jumpers (not recommended), or some low level CMC card Software/Firmware interrogation of the CMC card interface logic. With this information the CMC card logic behind the driver for the BUSMODE1# signal looks at the BUSMODE[4:2]# signals and drives the output in accordance to Table 6-6. At a minimum the CMC card logic shall decode the "Card Present Test" mode and one of the logical protocols modes from the BUSMODE[4:2]# signal encodings table. The CMC card shall inhibit its bus interface at all times except when a supported BUSMODE[4:2] mode is presented to it.