


ANSI/VITA 4.1-1996

Approved as an American National Standard by 

American National Standard
for IP I/O Mapping to VME64x

Secretariat

VMEbus International Trade Association

Approved March 3, 1998

American National Standards Institute, Inc.



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Approved March 8, 1998

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Abstract

This standard defines the mapping of the 50 user defined I/O pins from the IP (ANSI/VITA 4-1995) I/O connectors to VME64x boards' rear I/O connectors.

American National Standard

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Abstract

This draft standard defines the mapping of the 50 user defined I/O pins from the IP (ANSI/VITA 4-199x) I/O connectors to VME64x boards' rear I/O connectors.

Foreword

Since the introduction of IPs in 1988, most IP I/O—like that of the VMEbus—has been brought out on the board's front panel. Original VME had only 64 user defined I/O pins assigned for rear backplane I/O, and therefore was not possible to route the 200 IP I/O lines through a VME's rear backplane.

With the development of the VME64x (VME64 Extensions) Draft Standard, VITA 1.1-199x, 205 user defined I/O pin are now available for rear backplane I/O. It now is practical to route multiple IP's I/O through the VME64x backplanes. It makes sense to do this in a consistent method across all VME64x boards, backplanes and rear I/O transition boards.

The "good fit" between the 200 (typical count) IP I/O lines and the now-available 205 backplane I/O pins motivated the three sponsors of this draft standard to create a common, recommended pin assignment to promote interchangeability and competition within the industry, with more options and lower integration cost for integrators, VARs and end-users.

Chapter 1

Introduction

1.1 Introduction

This draft standard creates standard I/O pin assignment mappings between IP Mezzanine Modules (ANSI/VITA 4-1996 IP Modules) and VME64x (VITA 1.1-199x) boards' and backplanes' I/O pins.

Only I/O pin numbers are considered; the signals on these I/O lines may be input or output, digital or analog, or ground.

This draft standard applies only to VME64x boards that contain one or more IP mezzanine module positions. This draft standard does not directly apply to backplanes, enclosures, IP modules, nor I/O transition boards. This draft standard may indirectly impact the design and implementation of these system components.

Two pin assignment tables make up the bulk of the technical part of this draft standard. A set of observations to assist in reading the tables, and a set of rules for implementing the tables are also provided.

In addition to specifying I/O signal pin mapping in the tables, a certain number of power pins, both +5V and +3.3V are also assigned to the user defined I/O pins. This assignment permits, within some constraints, for transition modules to be powered through the VME64x boards via the backplane I/O connectors. Detailed specifications for this power, including choice of supported voltages, tolerances, maximum current, etc. are beyond the scope of this draft standard.

For convenience, several mechanical drawings showing relevant connector pin placements are reproduced here from other standards documents.

Hot swap capability and implementation is beyond the scope of this draft standard.

Impedance, resistance, maximum current carrying capacity, and crosstalk of the traces on the VME64x boards implementing the pin assignments in this draft standard are beyond the scope of this draft standard.

1.2 Abbreviations

The following abbreviations refer to the listed documents, above. Listed alphabetically.

2 mm connector	IEC 1076-4-101
IP	ANSI/VITA 4-1996
Original VME	ANSI/IEEE STD 1014-1987
VME64	ANSI/VITA 1-1994
VME64x	VITA 1.1-199x, VME64 Extensions Draft Standard

1.3 References

The following publications are used in conjunction with this draft standard. When a document is superseded by an approved revision (including draft standards), that revision shall apply. Listed alphabetically.

ANSI/VITA 1-1994	VME64 Standard, Approved April 10, 1995
ANSI/VITA 4-1996	IP Module Standard, expected approval August 1996
IEC 1076-4-101	2 mm High Density Connector
VITA 1.1-199x	VME64 Extensions Draft Standard, Draft 2.0, September 5, 1997

1.4 Standard Terminology

To avoid confusion and to make clear the requirements for compliance, many paragraphs in this draft standard are labeled with keywords that indicate the type of information they contain. This keyword usage is consistent with other VSO standards. The keywords are listed below:

- Rule
- Recommendation
- Suggestion
- Permission
- Observation

Any text not labeled with one of these keywords describes structure or operation. It is written in either a descriptive or a narrative style. The keywords are used as follows:

Rule <chapter>.<number>:

Rules form the basic framework of the Standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules shall be followed to ensure compatibility between board and backplane designs. Rules are characterized by an imperative style. The lower-case words "shall" and "shall not" are reserved exclusively for stating rules in this document and are not used for any other purpose.

Recommendation <chapter>.<number>:

Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in some awkward problems or poor performance. While the VME64x architecture has been designed to support high-performance systems, it is possible to design a system that complies with all the rules but has abysmal performance. In many cases a designer needs a certain level of experience in order to design boards that deliver top performance. Recommendations found in this standard are based on this kind of experience and are provided to designers to speed their traversal of the learning curve. All recommendations use the "should" or "should not" words to emphasize the importance of the recommendation. The "should" or "should not" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

Suggestion <chapter>.<number>:

A suggestion contains advice which is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some design decisions that need to be made in designing boards are difficult until experience has been gained. Suggestions are included to help a designer who has not yet gained this experience. Some suggestions have to do with designing boards that can be easily reconfigured for compatibility with other boards, or with designing the board to make the job of system debugging easier.

Permission <chapter>.<number>:

In some cases a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the

rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the "may" words to emphasize the importance of the permission. The lower-case "may" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

Observation <chapter>.<number>:

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They may also provide the rationale behind certain rules so that the reader understands why the rule must be followed.

Chapter 2

I/O Signal Mappings

2.1 Introduction

This chapter provides the required I/O signal mappings between the IP's I/O connector and VME64x rear I/O connectors.

2.2 Requirements

2.2.1 Mapping for VME64x 6U Boards

Rule 2.1:

VME64x boards conforming to this draft standard shall use the pin assignments given in the relevant tables.

Table 2-1
I/O Signal Mapping to VME64x P0 Connector

Connector	Position	Row						
		f	e	d	c	b	a	
P0	1	GND	D5	D4	D3	D2	D1	IP-D
P0	2	GND	D10	D9	D8	D7	D6	IP-D
P0	3	GND	D15	D14	D13	D12	D11	IP-D
P0	4	GND	D20	D19	D18	D17	D16	IP-D
P0	5	GND	D25	D24	D23	D22	D21	IP-D
P0	6	GND	D30	D29	D28	D27	D26	IP-D
P0	7	GND	D35	D34	D33	D32	D31	IP-D
P0	8	GND	D40	D39	D38	D37	D36	IP-D
P0	9	GND	D45	D44	D43	D42	D41	IP-D
P0	10	GND	D50	D49	D48	D47	D46	IP-D
P0	11	GND	C5	C4	C3	C2	C1	IP-C
P0	12	GND	C10	C9	C8	C7	C6	IP-C
P0	13	GND	C15	C14	C13	C12	C11	IP-C
P0	14	GND	C20	C19	C18	C17	C16	IP-C
P0	15	GND	C25	C24	C23	C22	C21	IP-C
P0	16	GND	C30	C29	C28	C27	C26	IP-C
P0	17	GND	C35	C34	C33	C32	C31	IP-C
P0	18	GND	C40	C39	C38	C37	C36	IP-C
P0	19	GND	C45	C44	C43	C42	C41	IP-C

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Table 2-2
I/O Signal Mapping to VME64x P2 Connector

Connector	Position	Row			
		d	c	a	z
P2	1	C47	B42	B41	C46
P2	2	C48	B44	B43	GND
P2	3	C50	B46	B45	C49
P2	4	B1	B48	B47	GND
P2	5	B3	B50	B49	B2
P2	6	B4	A2	A1	GND
P2	7	B6	A4	A3	B5
P2	8	B7	A6	A5	GND
P2	9	B9	A8	A7	B8
P2	10	B10	A10	A9	GND
P2	11	B12	A12	A11	B11
P2	12	B13	A14	A13	GND
P2	13	B15	A16	A15	B14
P2	14	B16	A18	A17	GND
P2	15	B18	A20	A19	B17
P2	16	B19	A22	A21	GND
P2	17	B21	A24	A23	B20
P2	18	B22	A26	A25	GND
P2	19	B24	A28	A27	B23
P2	20	B25	A30	A29	GND
P2	21	B27	A32	A31	B26
P2	22	B28	A34	A33	GND
P2	23	B30	A36	A35	B29
P2	24	B31	A38	A37	GND
P2	25	B33	A40	A39	B32
P2	26	B34	A42	A41	GND
P2	27	B36	A44	A43	B35
P2	28	B37	A46	A45	GND
P2	29	B39	A48	A47	B38
P2	30	B40	A50	A49	GND
P2	31	GND	3.3V	3.3V	3.3V
P2	32	VPC	5V	5V	GND

2.2.2 Observations

Observation 2.1:

Each table is organized to visually mimic the named physical backplane connector of the VME64x board. The visual rows and columns of the table correspond to the industry convention for naming the connector pin rows and the connector pin positions, respectively. Each entry in the table names the IP position and its I/O pin number that is electrically connected via traces on the VME64x board to the corresponding backplane pin in the table.

Pin positions for VME64x backplane connectors mounted on the VME64x board consist of a connector (**P1**, **P2** or **P0**), a lower-case **row** letter (**z**, **a**, **b**, **c**, **d** or **e**) and a **position** number (**1..32** or **1..19**).

The table entries in the form **A1**, **A2...D49**, **D50** refer to IP positions A through D and their respective IP I/O pin numbers 1 through 50.

Observation 2.2:

GND in a table entry for row f for 2 mm connectors means the board's ground plane, connected to the connector's ground shield.

GND in a table entry for VME64x P2 connector means the board's ground plane, connected to the connector's associated pin.

+5V means the +5 volt power plane, connected to the pins on the connector via the board. This +5 volt power must be connected to the system backplane +5 volt pins.

+3.3V means the +3.3 volt power plane, connected to the pins on the connector via the board. This +3.3 volt power must be connected to the system backplane +3.3 volt power pins.

Note that although the +5V and +3.3V pins are provided in this draft standard in order to power I/O transition boards, that different permitted system configurations may or may not actually provide power via these lines.

Observation 2.3:

If only P0 is available for IP I/O, then all of IP-D and nearly all of IP-C [pins 1..45] I/O lines may be routed to P0 pins only.

Observation 2.4:

If rows **a** and **c** of P2 are used for another function, then all of IP-D, all of IP-C and most of IP-B [pins 1..40] I/O lines may be routed to available backplane pins.

Observation 2.5:

The pin assignment of IP-A matches the pin assignment in two rows of original 50-pin flat ribbon cable. This assignment may be useful for optimizing signal to noise or crosstalk for some products.

Observation 2.6:

The **GND** and **VPC** table entries in **Row z**, and the **GND** table entries in **Row d** are part of the VME64x Draft Standard.

2.2.3 Rules and Permissions

Rule 2.2:

VME64x boards conforming to this draft standard shall use the connector pin and IP position conventions contained in the underlying relevant standards (identified in the other documents section above).

Rule 2.3:

VME64x boards conforming to this draft standard containing four IP positions shall label them A, B, C, and D.

Permission 2.1:

Boards containing fewer than four IP positions may select a subset of {A, B, C, D}.

Rule 2.4:

For each labeled IP position, its I/O lines shall be connect to the corresponding labeled pins in the tables.

Observation 2.7:

Permission 2.1 says that an IP Carrier Board may have any number of IPs, but that the labels are to correspond to the labels contained in these tables. In practice, this may mean that the IP label is dictated by the choice of which backplane connectors are used for IP I/O.

Rule 2.5:

VME64x boards conforming to this draft standard shall connect +5 volt system power and +3.3 volt system power to the identified pins in the tables.

Rule 2.6:

VME64x boards that implement a subset of the pin assignments given in this draft standard shall NOT claim conformance to this draft standard UNLESS it is clearly stated, in every relevant place, "COMPLIANT with a SUBSET of VITA 4.1-199x Pin Assignments." The word, "SUBSET," shall be capitalized.

Permission 2.2:

Fuses or similar protection devices are permitted in the +5 and +3.3 power lines. The power is permitted to be switched, as well as protected, if desired.

Permission 2.3:

VME64x boards conforming to this draft standard may use P2 rows **a** and **c** for purposes other than IP I/O pin assignments. Or, VME64x boards may use P2 rows **z** and **d** for purposes other than IP I/O pin assignments.

Permission 2.4:

IP pins may be connected to other connectors, or to other electronics on the IP Carrier Board, besides those given in this draft standard.

Permission 2.5:

Any subset or all IP I/O pins may be mechanically or electrically disconnectable from the corresponding backplane pin provided that the default condition is connected.

Chapter 3

Reference Figures

3.1 Introduction

Figure 3-1 illustrates a possible layout and orientation of the IP I/O connectors on a VME64x board. The figure is not to scale, and does not show required positions. Only the IP I/O connectors, not the IP logic connectors are shown. The view is the normal, component side view of the VME64x board, with the backplane on the right and the front panel, not shown, on the left.

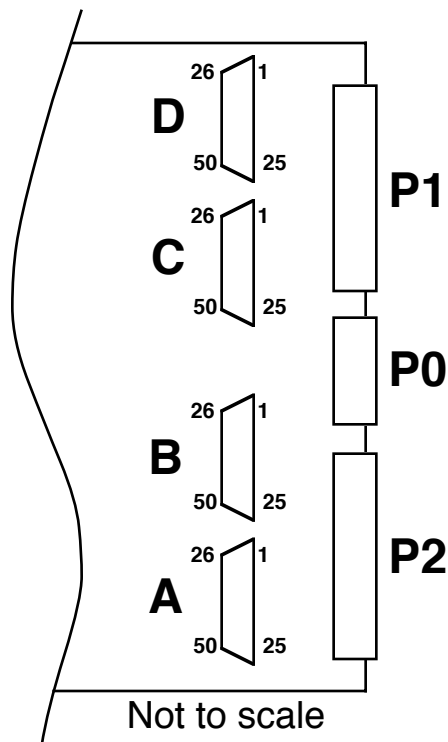


Figure 3-1 Possible IP Connector Layout on a 6U VME64x Board