

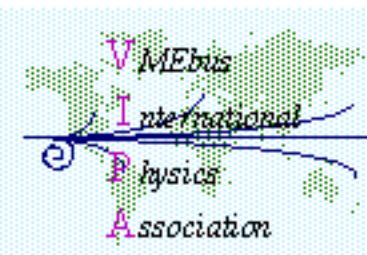
System level live insertion

Jan Buytaert

Live insertion: definition & aims

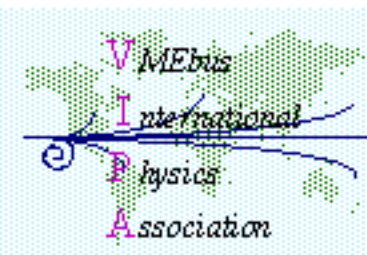
- “Ability to **insert/withdraw** a system board component, while the system is powered and operating, **without causing a system upset or damage**”
- Aim: maximize system availability (“Uptime”)
- Goal: self-completing process
- Covered by
 - VITA 1.4 VME64x Live Insertion System Requirements (Draft document)

Problem analysis & solutions.



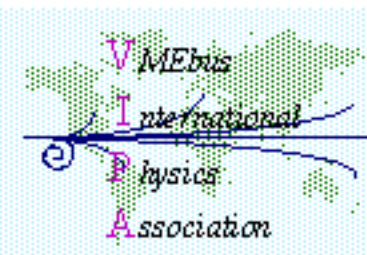
- “...insert/withdraw...”
 - On-line board replacement, system expansion, configuration change.
- “...without causing a system upset or damage.”
 - Mechanical interference with adjacent boards.
⇒ Solder(top)-side covers.
 - ESD ⇒ ESD-protection.
 - Bus corruption (ongoing traffic, spurious interrupts or bus request,...) ⇒ pre-charge and HighZ bus pins (ETL).
 - Insert in daisy-chains (BG, IACKin/out) ⇒ LI/O*
 - Power glitches ⇒ Power control circuitry (LI/O*)
 - reconfigure system to include/exclude resource changes.
⇒ CR/CSR (board configuration data and capabilities)

Power control.



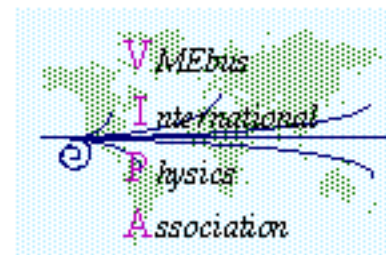
- Isolate board load from bus supplies (power MOSFET's, $\Delta V_{on} < 2\%$)
- Manual control
 - Front-panel toggle switch
 - Microswitch in handles (recommended)
- Remote control
 - Precedence over manual control
 - P1 LI/I*:
 - low = power-down
 - Open-collector with on-board pull-up (backward compatibility)
- Limit ramp-up/down current $< 2 \text{ A/ms}$

Daisy-chain . . .



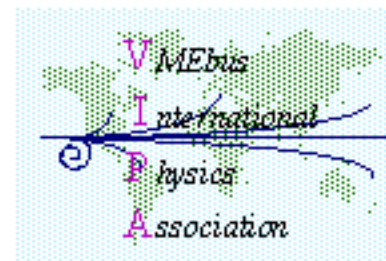
- **LI/O* asserted** when board (including interface) is fully configured and ready for normal operation
- Active jumpering circuit required
 - distributed (backplane mounted bypass circuit?)
 - or centralized (dedicated module module?)

Visual indicators



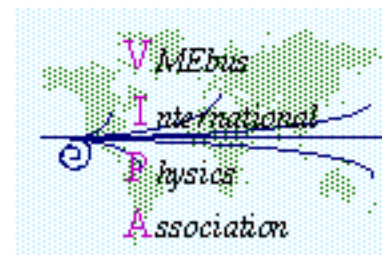
- **INACTIVE** (power down)
- **RUNNING** (normal operation)
- when both lit == error condition

System reconfiguration



- Normally system is informed of planned change
 - Removal
 - System Host gracefully shuts down operation
 - resets module and I/O
 - and powers it down
 - Insertion
 - Host system powers it on
 - Resets
 - Executes self-test
 - Configures board
 - Enables bus interface

System reconfiguration (2)



- Awareness of **unsolicited** presence/disappearance
 - Polling (read) in CSR space. Slave (even in reset state) should respond with geographic address value
 - High priority level interrupt generated when manual power off is detected
- “Bus error catching” utility
 - detects excessive delays before time-outs occur (polling!)
 - latches bus address and generates interrupt
- SW - monitoring, downloading drivers, ...
- Considerations: I/O (tri-state), user power pins, etc.