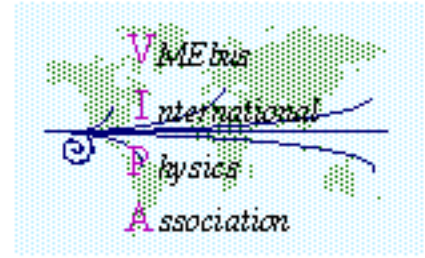
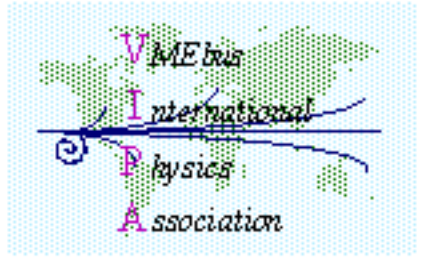


VME64xP
Rules
Recommendations
Features
etc.

Robert Downing

Address & Data

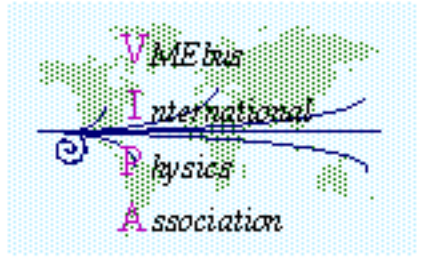


- Address Recommendations
  - A32 and A64
  - Latch Addresses
- Data Rule
  - D32
- Data Recommendation
  - D64

AM Codes - Recommended

• A24	2F	D32 CR/CSR Space
• A32	08	D64 MBLT
	09	D32 Single
	0B	D32 BLT
	20	D64 2eVME
• A64	00	D64 MBLT
	01	D32 Single
	03	D32 BLT (preferred)
	20	D64 2eVME

CSR Registers

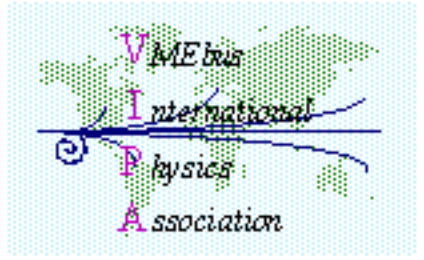


- Required Base Address Register (BAR)
  - See VME64, Section 2.3.12; VME64x, Section 3.2.11
  - Load BAR with Geographical Address at power-on or any board reset
  - BAR accessed with A24
- Conditional Requirements
  - User Space pointers, see Table 3.3.3-1; see VME64x, Section 10.2.1.3
  - Address Relocation, see VME64x, Table 10.13
- Bit Flag required if Module issues BERR*
  - See VME64x, Chapter 10; Bit 3 of CSR Bit Set and Bit Clear Registers

CR Registers

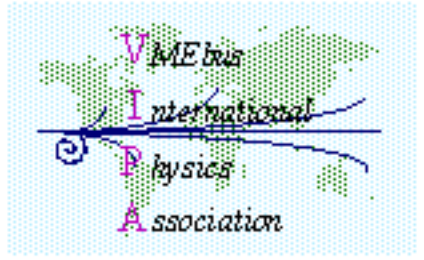
- Required CR's
  - See Table 3.3.2-1; VME64, Section 2.3.12: VME64x, Chapter 10.
  - All but one from VME 64 and VME64x
- Require Master or Slave characteristics and Capabilities Registers
  - See Table 3.3.2-2 and VME64x, Section 10.2.1.3
- Require that certain other registers - if implemented - be in certain locations
  - See Table 3.3.2-3 and 3.3.2-4

Why Standard Registers?



- Software, Software, Software
- Most large systems have at least one processor in each subrack
- Necessary for “Plug-and-Play”
  - Not real P & P, but helps diagnostics and setup
- Future VME enhancements
  - Hard to predict with certainty, however, these are a start

Mezzanine Recommendations



- PMC
  - Higher speed uses
  - Backplane mapping per IEEE P1386
    - one PMC map to P2, rows a&c
    - two PMC map to P2, a & c and d & z
- IP
  - Lower speed uses
  - Backplane mapping per VITA 4.1-199x
  - Conflicts to be aware of:
    - VME64xP P0 conflicts with 4.1 and 1386 use of P0
    - P2 pinout in 4.1 does not conflict