P0
VME64xP issues

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Jo User Pin Specifications (1)

- 2 mm hard metric connector, 5(+2shield) rows
- VME64x leaves all 95 pins user defined. (Outer shield-rows to GND)
- VME64xP defines some pins for: (see 6.3.2)
  - power
    - +5 V for 9U (6 pins)
    - 4 configurable voltages Vx,Vy,Vw,Vz (8 pin) + returns (8 pins)
    - power feed-through's for PTM's : +/-V1FB, +/-V2FB (4 pins)
    - 4 Power Code for rear PTM's : PC[0..3] (4 pins)

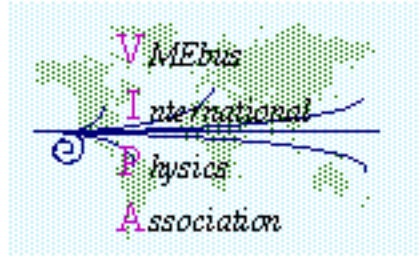
Jo User Pin Specifications (2)

- Bussed signals
  - 4 Differential terminated buses TBUS1+/- ...TBUS4+/- for balanced PECL signals (8 pin)
  - 2 Wire-Or Buses TBUS OC1,2 (2 pins)
- Non-bussed signals
  - 2 reference voltages for Analog Power AREF_WX,AREF_YZ (2 pins)
- User defined (39 pins)

J0 User Pin Assignment

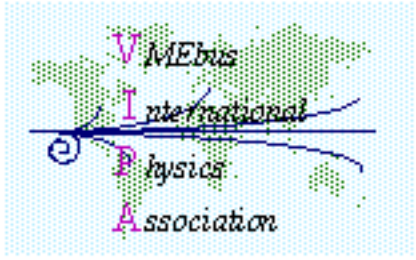
Pin #	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	COM	+5V	+5V	+5V	+5V	+5V	COM
2	COM	RET_WX	RESERVED	+5V	TBUS1+	TBUS1-	COM
3	COM	RET_WX	RESERVED	RESERVED	TBUS2+	TBUS2-	COM
4	COM	Vw	RESERVED	USER I/O	USER I/O	USER I/O	COM
5	COM	Vw	RESERVED	USER I/O	USER I/O	USER I/O	COM
6	COM	RET_WX	RESERVED	USER I/O	USER I/O	USER I/O	COM
7	COM	AREF_WX	RESERVED	USER I/O	USER I/O	USER I/O	COM
8	COM	RET_WX	RESERVED	USER I/O	USER I/O	USER I/O	COM
9	COM	Vx	RESERVED	USER I/O	USER I/O	USER I/O	COM
10	COM	Vx	RESERVED	USER I/O	USER I/O	USER I/O	COM
11	COM	Vy	RESERVED	USER I/O	USER I/O	USER I/O	COM
12	COM	Vy	RESERVED	USER I/O	USER I/O	USER I/O	COM
13	COM	RET_YZ	RESERVED	USER I/O	USER I/O	USER I/O	COM
14	COM	AREF_YZ	RESERVED	USER I/O	USER I/O	USER I/O	COM
15	COM	RET_YZ	RESERVED	USER I/O	USER I/O	USER I/O	COM
16	COM	Vz	RESERVED	USER I/O	USER I/O	USER I/O	COM
17	COM	Vz	RESERVED	RESERVED	TBUS3+	TBUS3-	COM
18	COM	RET_YZ	RESERVED	RESERVED	TBUS4+	TBUS4-	COM
19	COM	RET_YZ	RESERVED	RESERVED	TBUS_OC1	TBUS_OC2	COM

Configurable voltages
Vw, Vx, Vy, Vz



- Great flexibility
- Need proper keying for protection!
- Can be bussed (e.g. VIPA backplane)
- or unbussed (e.g. rear PTM) or partly
- Typical configuration defined
  - High power ECL = -5.2V, -5.2V, -5.2V, -2V

Power transition modules (PTM)

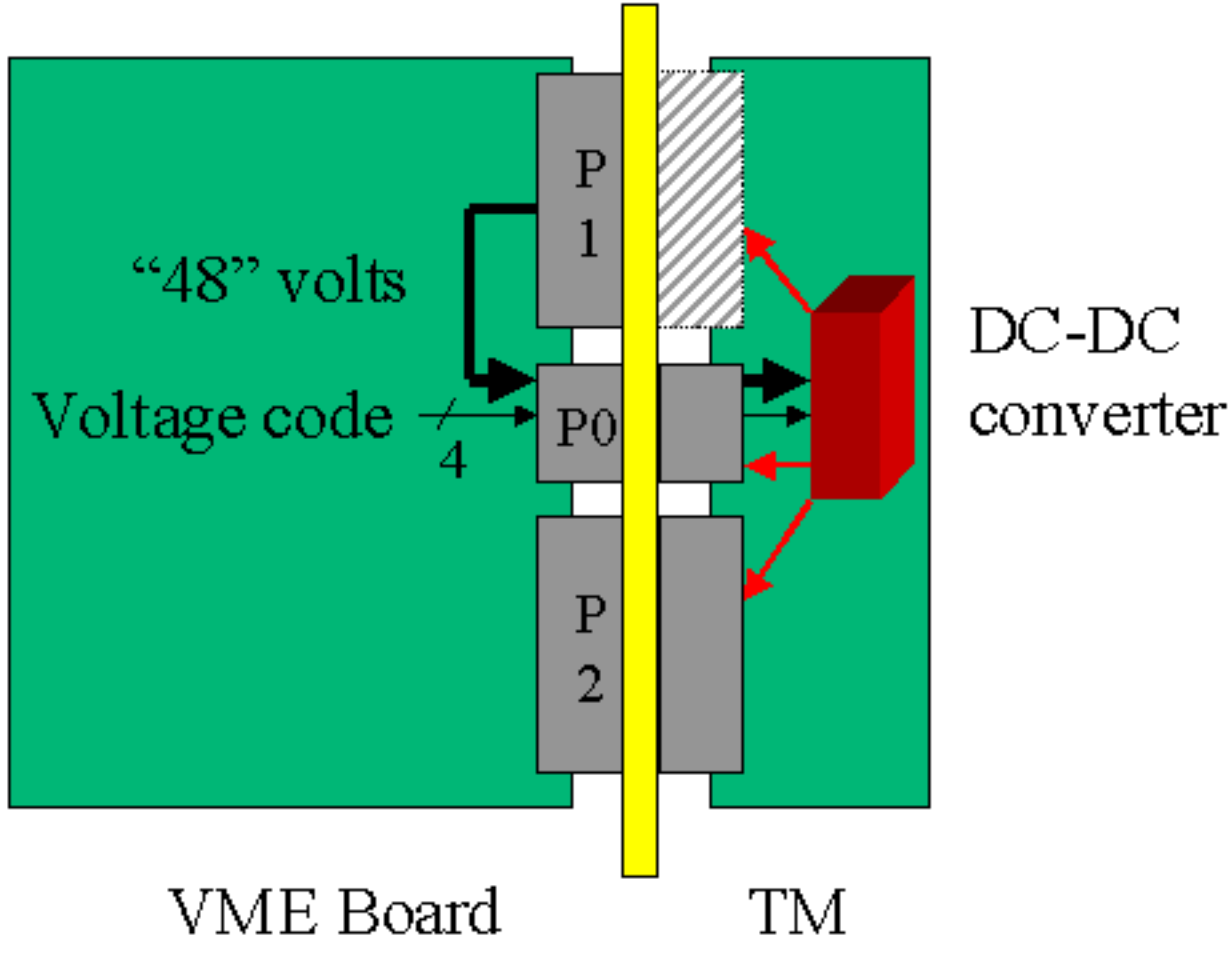


- Pure VME64xP (see 4.7)
- Transition Module carries DC-DC Converter
  - Saving main board space, less noise(backplane acts as shield)
- Primary DC-DC power
  - Fed to it via front board (+/-V1FB, +/-V2FB = 48V floating)
- Code pins (PC0...3) determine voltages Vw,Vx,Vy,Vz
  - If PTM does not support code, then no power-up
  - One PTM could support several codes
  - Coded by GND connection on VME board

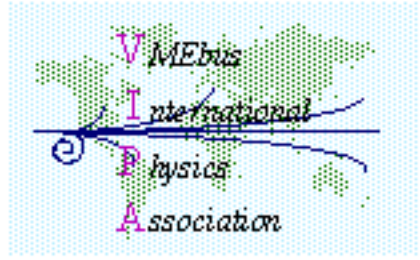
PTM (2)

- Current codes
  - 0xF (no board installed)
  - 0x0 (powered-off board installed)
  - 0xE (High power ECL)
  - All others reserved
- Can be used instead of bussed voltages
  - For low power applications
  - Customized power per individual slot (special boards)
  - Cost-effective when few boards need Vw,x,y,z. (ECL power)
- Cooling (air flow)
- Not yet designed (volume may be possible)

PTM schematically



P0/Jaux and Paux/J0 adapters



- Mechanical adapters
- Aimed for
  - New VME64xP board developed in “Jaux crate”
  - existing Paux boards to function in new VME64x(P) subrack
- Minimal depth (boards stick out by ~ 3cm)
- Under development in CERN/EP/EDO
- Power not identical
    - Jaux -5.2, -2, +15, -15
    - J0 (VME64xP) -5.2, -2, (+15,-15 missing from rear PTM)