6 Trends and New Developments for Pixel Detectors

Abstract Present trends in research and development on pixel detectors for future particle detectors and new imaging systems are described. The hybrid pixel technology can be viewed as the state of the art of pixel detectors today. Its further potential and its limitations are reviewed. Monolithic pixel detectors which integrate the detection sensor and the readout electronics are attractive but also challenging. Their development as seen today and compromises to be made are discussed.

6.1 Introduction

In particle physics pixel detectors have just begun to be built for large-scale applications, such as vertex detectors in collider experiments. The other, rather complementary field for pixel detectors is their use in imaging applications, most notably biomedical imaging with very different requirements and limitations [289]. In particle physics experiments individual charged particles, usually triggered by other subdetectors, must be identified with high demands on spatial resolution and timing. In imaging applications the image is obtained by the untriggered accumulation (integrating or counting) of the quanta of the impinging radiation, often also with high demands on rate (e.g. \( \geq 1 \text{ MHz per pixel in certain radiography or CT applications} \)) and on imaging resolution (\( \geq 10 \text{ line pairs/mm} \)) and contrast.

Pixel detectors in high energy physics typically have signal charges in the order of at least 8,000 electrons in worst case scenarios including charge sharing and radiation damage effects. As described in Sect. 5.3, imaging applications often require efficient detection of signal charges almost an order of magnitude lower than this. The spatial resolution of pixel detectors is governed by the attainable pixel granularity. Resolutions of about 10\( \mu \text{m} \) are obtained with pixel cell dimensions in the order of 50–100\( \mu \text{m} \). The requirements from radiology (mammography) are similar or even less demanding, while some applications in autoradiography require submicrometer resolutions, not attainable with the present day pixel detectors. For applications with lower demands on the spatial resolution (\( \approx 10 \mu \text{m} \)) but with demands on real-time and time-resolved data acquisition, semiconductor pixel detectors are however very attractive.
Thin detector assemblies are mandatory for the vertex detectors at collider experiments, in particular for the planned linear $e^+e^-$ collider. While silicon is an almost perfect material for particle physics detectors, allowing the shaping of electric fields by tailored impurity doping, the need of high photon absorption efficiency in radiological applications requires the study and use of semiconductor materials with high atomic charge, such as GaAs or CdTe (see Chap. 2). For such materials the charge collection properties are much less understood and mechanical issues, in particular those related to hybrid pixels, exist abundantly, for the hybridization of detectors especially when they are not available in wafer scale sizes. Last but not least, the cost–performance ratio is an important factor to consider if an imaging application could be commercially interesting.

### 6.2 Limitations and Prospects of the Hybrid Pixel Technology

The hybrid pixel technology has been the pixel technology of choice for the next generation of detectors in high energy physics at the LHC and in high-rate fixed target experiments. This choice is governed by the fact that this technology is the only one which at present is sufficiently mature to build detectors with an area larger than a few square centimeters. The main advantages of this technology for large-scale detectors are the following:

- The hybrid assembly approach allows testing at several intermediate steps, thus offering a comparatively high yield in producing pixel modules with area sizes of tens of square centimeters.
- The chip, sensor, and interconnection technologies are industrial processes, matured during many years of experience. They are available from a variety of industrial vendors.
- Because the sensor and the amplifying/readout chip are separate items, materials other than silicon can be used for the sensor substrate.

The disadvantages of the hybrid technique become evident when one addresses the requirements of particle detectors at high-energy accelerators of the future, in particular the demands on high resolution in high-multiplicity environments (i.e. small cell size), on a low material budget, and on high speeds.

The technological limitations are mostly related to the bumping technology and the power density associated with the constraint that the electronics circuitry for amplification and logic is confined to the same area as the detecting electrode. In 0.1 $\mu$m CMOS technology the projected pixel size could be as small as $10 \times 80 \mu$m² or $25 \times 25 \mu$m² for a square geometry. This leads to an estimated power density of 30 mW/mm² or 30 kW/m² detector.

The pitch for the PbSn bumping technology is limited to about 10–15 $\mu$m due to mask alignment and galvanic process precision [328]. In the case of
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Indium bumps the smallest pitch obtained so far is 15 µm \([329]\). The technological limit lies below 10 µm.

For LHC upgrade scenarios pixel detectors are also discussed for larger area coverage than today. In this case, the present hybrid pixel technology with one-to-one coverage of the area with sensor, readout chips, and a module interconnect layer (flex) not only constitutes a significant material issue but also drives the costs of pixel detectors at larger radii, and solutions must be found.

6.2.1 MCM-D Integration

With decreasing pixel cell sizes the high-density interconnection techniques become more complex, demanding more advanced technologies. A development for the next generation of hybrid pixel detectors regarding the power and signal distribution in a module is the so-called multichip module technology deposited on silicon substrate (MCM-D) \([330]\). This concept has been contrasted with the flex-hybrid approach for module hybridization in Fig. 4.13. Another illustration is shown in Fig. 6.1 which stresses the possibilities of

![Diagram of MCM-D integration](image-url)

Fig. 6.1. (a) Cross-sectional view of a full hybrid pixel module with wire bonding from the readout chip to the flex kapton layer. (b) Cross section of the edge of a readout chip at the transition between the active detection area (right) and the outer periphery (left) in the MCM-D concept. In the periphery outside the active area the power bus lines are routed in four metal layers which are built up directly on the sensor substrate. In the active area the layers are simply crossed by vias to the chip side where bump bonding is done \([330]\).
the MCM-D technology with respect to the extra degrees of freedom for the routing of power lines [331].

The MCM-D concept offers an elegant way to integrate ICs and sensors into a quasi-monolithic high-density-interconnect module. A multiconductor-layer structure is built up on the silicon sensor itself. Layers of a dielectric (e.g. photosensitive benzocyclobutene [BCB], $\varepsilon_r = 2.7$) and metal (Cu) are deposited and patterned on the electrode (i.e. pixel) side of the sensor by using thin-film technologies. In the process presented in [330], BCB is spun on the silicon sensor with a thickness of $6 \mu m$, while Cu is electroplated with $3 \mu m$ thickness. The processing temperature resides below $220^\circ C$ at all times and has been proven not to compromise the sensor characteristics. The metal layers are connected by vias of $25 \mu m$ minimum diameter. Finally, the same bumping and flip-chip processing as described in Chap. 4 is applied to connect the front-end ICs to the sensor elements. Figure 6.2 shows scanning electron microphotographs of via structures made with MCM-D technology. In the displayed example four metal layers are built up from the silicon sensor substrate.

![Fig. 6.2. (a) Scanning electron microphotograph of an MCM-D vias structure. (b) Cross section cut with a bump-bond connection to the readout chip. (Courtesy of Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, IZM, Berlin)](image-url)

The MCM-D techniques allow one to make compact modules in which all pixels have equal sizes, even those which lie between chip boundaries, due to the increased routing freedom. Furthermore, the bus structures and the voltage supply lines can be buried in several layers under the inactive area at the edge of the module. The feed-through via system to the readout chip, which is necessary for every pixel cell, is shown in Fig. 6.1b. Since sensor and chips must cover the same area, the size of the sensor is wider for the same readout chip width than in the flex-hybrid concept and also longer in order to house, for instance, a module control chip and other necessary passive components for supply bypassing (see Fig. 6.3). Yield losses apply to the entire module. Therefore the yield requirements on MCM-D pixel
modules are very high. In return, the MCM-D technology can provide a compact multichip pixel module without external wire bonds [35] and flex circuitry. Using the ATLAS readout electronics several prototype MCM-D modules with 16 front-end chips have been built with good and encouraging preliminary results [35,331], showing that complex MCM-D modules can be built with negligible increase in noise performance. At present, yield and perhaps cost issues are the limiting factors of the MCM-D technology for large pixel detectors.

6.2.1.1 Sparse CMOS Using MCM-D

The integrated multilayer possibilities provided by the MCM-D technology can, in the future, allow much wider applications than sketched above. The increased flexibility having become available in PCB technology after the introduction of the multilayer techniques is in principle also expected here. One such application for imaging can be the use of the MCM-D multilayer structure to fan out chip I/O lines to larger sensor pixels as sketched in Fig. 6.4. In many X-ray applications, for example, the optimal pixel pitch and cell size of the image-taking sensor is much larger than the required pixel area for the chip circuitry, especially with the advancement of very small scale CMOS processing technologies. An ≈1-cm² chip can be used for readout of a much larger area. This might also be interesting for large area pixel detectors in high energy physics as the smaller number of readout chips per module offers a price reduction in places where a less precise position resolution is sufficient. However, special attention must be given to the additional capacitance introduced by the fan-out lines, which can be much larger than the actual pixel capacitance.

6.2.2 Interleaved Hybrid Pixels

An approach to cope with the pitch limitations of the hybridization process exploits capacitive coupling of the pixels to have a larger readout and
bump-bonding pitch than the actual sensor pixel pitch. This has been directly adopted from silicon microstrip detectors [332, 333] for which integrated capacitive charge division readout is very often employed to reduce the number of readout channels. The development is carried out in the context of pixel detector R&D for a linear collider detector under the label HAPS (hybrid active pixel sensors) [334, 335]. Figure 6.5a shows a layout of a pixel matrix with readout and sensor pixels at a different pitch. Every pixel is biased via a polysilicon resistor, but only a fraction of pixels is read out.

Figure 6.5b is the result of the obtained spatial resolution when the device is scanned with a fine focus laser. Charge sharing between neighboring pixels through their interpixel capacitance improves the space resolution for a HAPS device with a pixel pitch of 100 µm and readout pitch of 200 µm by roughly a factor of 4 compared to the binary pixel pitch/√12 resolution. Values between 3 µm at the interleaved pixels (maximum charge sharing) and 10 µm at the readout pixel (minimal charge sharing) have been obtained (Fig. 6.5). This level of improvement can be extrapolated to small pixel pitches of

**Fig. 6.4.** Layout of a sparse CMOS fan-out routing
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20–25 µm provided a signal-to-noise ratio (S/N) >100 is maintained and the charge loss into neighboring pixels is less than 50% [334]. Needless to say that the interleaved pixel concept imposes lower constraints on the bumping process and reduces the total power consumption, when comparing to a device with amplification electronics for every pixel cell, of course on the expense of a degraded two-track resolution and the necessity for analog pulse height readout.

6.2.3 Active Edge Three-Dimensional Silicon Pixel Detectors

The features of doped silicon allow interesting geometries with respect to field shapes and charge collection. The so-called three-dimensional silicon detectors have been proposed [153] to overcome several limitations of conventional silicon pixel and also silicon strip detectors, in particular in high-radiation environments or applications which require a large active/inactive area ratio [288]. Examples are detectors which must operate close to particle beam lines and for which the radiation environment produces particle fluences in excess of $10^{15}$ particles/cm², with the additional complication that the irradiation is not homogeneous over the detector. The large active/inactive area ratio is of great advantage, e.g. for applications using Bragg diffraction with synchrotron light (see Sect. 5.2) where number and intensity of many Bragg spots need to be detected with high efficiency.

As shown in Fig. 6.6a, a three-dimensional structure is obtained by processing the n⁺ and p⁺ electrodes into the detector bulk rather than by conventional implantation on the surface by combining VLSI and MEMS (micro-electro-mechanical systems) technologies. Charge carriers are drifting inside the bulk parallel to the detector surface (Fig. 6.6b) over a typical drift distance of 50 µm. Another feature is the fact that the edge of the sensor can be a collection electrode itself [336], thus extending the active area of the sensor to within about 10 µm to the edge. This results from the undepleted depth at this electrode. Edge electrodes also avoid inhomogeneous fields and
Fig. 6.6. (a) Schematic view of a three-dimensional silicon detector, (b) charge collection in a three-dimensional silicon structure and (c) in a conventional planar electrode detector, (d) a structure combining three-dimensional and planar features.
surface leakage currents which usually occur due to chips and cracks at the sensor edges (Fig. 6.6c). The main advantages of three-dimensional silicon detectors are summarized in Table 6.1. They mostly come from the fact that the electrode distance is short (50 µm) in comparison to conventional planar devices at the same total charge, resulting in a fast (1–2-ns) collection time, low (<10 V) depletion voltage, and, in addition, a large active/inactive area ratio of the device. Note, however, that the three-dimensional electrodes inside the bulk volume constitute regions of dead area themselves.

Table 6.1. Comparison of characteristic properties of three-dimensional silicon detectors and standard planar detectors

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<th>Three-dimensional detector</th>
<th>Planar detector</th>
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<tr>
<td>Charge collection path</td>
<td>50 µm</td>
<td>300 µm</td>
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<tr>
<td>Depletion voltage</td>
<td>&lt;10 V</td>
<td>70 V</td>
</tr>
<tr>
<td>Charge collection time</td>
<td>1–2 ns</td>
<td>10–20 ns</td>
</tr>
<tr>
<td>Edge sensitivity</td>
<td>&lt;10 µm</td>
<td>500 µm</td>
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</table>

The technical fabrication of three-dimensional silicon detectors is more used than planar processes and requires a bonded support wafer as well as reactive ion etching of the electrodes into the bulk. A compromise between three-dimensional and planar detectors, the so-called planar–three-dimensional detectors [337], maintaining the large active area, is shown in Fig. 6.6d. Planar technology is used, but edge electrodes are included, fabricated by diffusing the dopant from the deeply etched edge and then filling it with polysilicon. Prototype three-dimensional and planar–three-dimensional detectors using strip or pixel electronics have been fabricated. The three-dimensional detectors show encouraging results with respect to speed (3.5-ns rise time) and radiation hardness (>10^{15} protons/cm²) [338]. Figure 6.7 demonstrates the achievable energy resolution (σ_{E}/E = 2%) observed in a measured ²⁴¹Am spectrum.

6.3 Monolithic and Semimonolithic Pixel Detectors

Because detector and readout electronics circuitry are in many fields of applications made of silicon as the base material, the idea of monolithic rather than hybrid devices is very appealing. They offer the possibility of very low input capacitances and hence very low noise figures, avoiding at the same time the costly and complex hybridization process. Several attempts were made in this direction in the 1980s [340–343]; however, the developments have so far been limited to small prototype devices. No real particle or radiation detector has emerged. Today, the situation regarding monolithic devices is still unchanged.
Several developments look promising but still need to prove essential characteristics needed for high-energy particle detection, most notably the radiation tolerance. In this section some of these new concepts are introduced. The borderline between truly monolithic pixels, where sensor and amplification and readout circuitry are one entity, and semimonolithic devices, where some hybridization is still necessary, is not well defined. Hybrid pixels use electronic circuitry in every pixel cell with hundreds of transistors. In monolithic devices the maximum number implemented so far are 15 transistors [344], allowing only a simple logic implementation. Further signal treatment is deferred to the outer frame of a pixel matrix.

As to the ultimate goal to implement standard VLSI CMOS circuits on a high resistivity, fully charge collecting substrate material, the present compromises can be classified into:

- Nonstandard CMOS on high-resistivity bulk
- Standard CMOS with charge collection in an epitaxial silicon layer
- CMOS on SOI (nonstandard)
- Amorphous silicon on standard CMOS ASICs
- Amplification transistor implanted in high-resistivity bulk

The development of monolithic pixel devices has been challenged anew by the demands of future collider experiments, most notably linear $e^+e^-$ colliders [345], where very little material ($\ll 1\% X_0$) per layer, small pixel sizes
(≈20 × 20 µm²), and high rate capability (80 hits/(mm² ms)) is required. This is due to the very intense bremsstrahlung of narrowly focused electron beams close to the interaction region which produce electron–positron pairs in vast numbers. Readout speeds of 50 MHz (row clocking rate) and full detector frame readout times of the order of 40 µs are required.

6.3.1 Monolithic Pixels on Bulk Silicon

The first successful development of a monolithic pixel detector prototype which could already be used as a particle beam telescope was made as early as 1992 [343, 346, 347]. As an historical achievement this development has already found its mentioning in Chap. 1. The device is based on a high-purity, high-resistivity p-type bulk PIN diode of which the junction is created by an n-type diffusion layer. On the top, an array of ohmic contacts to the substrate serves as collection electrodes. A schematic cross-sectional view is shown in Fig. 6.8. The circuitry on the top controls the readout of the pulse height information from each pixel cell to the off-shell electronics and consists of nine PMOS transistors. The diode junction is formed on the backside. The charge-collecting electrodes therefore sit in a region of minimal electric field when the device is operated in full depletion. Almost 90% of the sensor area is taken up by an n-well containing PMOS circuitry and at the same time serving as a shield between the bulk and the PMOS transistors. Note that

Fig. 6.8. Cross section of an early developed monolithic pixel detector [347]
no NMOS transistors can be implemented in the active area and that a dead area is introduced at the border of the device where the readout circuitry is placed.

An array of $10 \times 30$ pixels with $125 \times 34 \, \mu m^2$ pixel cells has been realized and characterized in a high-energy muon beam using a telescope arrangement of four-pixel arrays. Figure 6.9 shows an event display of the four planes passed by an ionizing high-energy muon. An S/N (single channel) of 55 was observed with a spatial resolution $\sigma$ of $2.2 \mu m$ in the short $34\mu m$ pixel direction.

Fig. 6.9. Event display showing the passage of an ionizing track through four planes of a monolithic pixel detector [347]

While the achieved results were truly spectacular at this early stage of pixel developments, no large-scale detectors evolved from this approach mostly due to the use of nonstandard processing technologies.

6.3.2 Monolithic CMOS Pixels

Commercial CMOS technologies use low-resistivity silicon which is not suited for charge collection. However, in some technologies an epitaxial silicon layer of a few to $15 \mu m$ thickness can be used—[348–351]. The generated charge is kept in the epitaxial layer by potential wells at the boundary and reaches an n-well collection diode by thermal diffusion. The signal charge is hence very small ($<1000e^-$) and its time development is inherently slower ($\approx 100 \text{ns}$) than that obtained in detectors with a highly resistive, depleted bulk. Very low noise electronics is required for this development. The principle of a monolithic active pixel sensor (MAPS) is shown in Fig. 6.10. CMOS pixels are potentially very cheap particle detectors, as standard processing technologies are used. But, despite the use of CMOS technologies, only NMOS transistors are allowed in the active area because of the n-well/p-epi collecting diode which does not permit other n-wells.

The fundamental difference between CMOS monolithic active pixel sensors and CMOS camera chips is that the former must have a 100% fill factor for efficient particle detection. Standard commercial CMOS technologies are used which have a lightly doped epitaxial layer between the low-resistivity
Fig. 6.10. Schematic cross section of a CMOS pixel detector cell (MAPS). The charge is collected in an n⁺-well diode on the p-epitaxial layer [350].

silicon bulk and the planar processing layer. The thickness of the epitaxial layer depends on the detail of the CMOS process technology. It can be at most 15 µm thick and not every CMOS process possesses an epitaxial layer. Different developments using similar approaches exist on both sides of the Atlantic [351–355]. Prototype detectors have been produced in 0.6, 0.35, and 0.25 µm CMOS technologies [344, 356].

The MAPS structure (Fig. 6.10) is depleted only directly under the n-well collection diode where full charge collection is obtained; the collection is incomplete in most parts of the epitaxial layer. Figure 6.11a shows the response to X-ray photons from a $^{55}$Fe source at energies of 5.9 and 6.5 keV. The peaks correspond to photons absorbed in the small depleted region under the n-well. The main part of the spectrum, however, corresponds to the absorption of photons in the undepleted part of the epitaxial layer. A chip submission using a process with no epitaxial layer, but with a low doped substrate of larger resistivity has also been tried (MIMOSA-4) [358]. The fabricated devices proved to function with high detection efficiency for minimum ionizing particles. While a complete abstention from the epitaxial layer is not a solution for CMOS pixels as particle detectors, this observation renders the uncertainty in and the need of an epitaxial layer with substantial thickness less constraining.

Matrix readout is performed using a standard three-transistor circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices (see Fig. 6.11b), but can also include current amplification and current memory [344]. For an image two complete frames are subtracted from each other (correlated double sampling) which suppresses switching noise. Noise Figs. of 10–30 e⁻ and $S/N \approx 20$ have been achieved [344] with spatial
Fig. 6.11. (a) Response to a $^{55}$Fe 5.9-keV X-ray source [357]. An interpretation is given in the text. (b) Matrix operation of MAPS monolithic pixels.

resolutions below 5 $\mu$m. In particle detection, two successive frames of a CMOS matrix are taken and subtracted [344, 352] (correlated double sampling). From this the hit signal is obtained by a further pedestal frame subtraction.

The radiation hardness of CMOS devices is a crucial question for particle detection at high-intensity colliders. MAPS appear to sustain non-ionizing interaction damage up to $\approx 10^{12}$ $n_{eq}$ [355, 359] and higher [360], while the
damage effects of $\gamma$-rays and ionization from charged particles are not yet completely understood for the time being [358]. At a linear $e^+e^-$ collider, radiation doses in the order of several kilograys, mostly from ionizing electron–positron pairs, are expected [345]. Irradiation of CMOS pixel devices with 10-keV X-rays to 2 kGy shows a degradation in S/N of about 15–20% [358], which appears to be close to being sufficient for this application.

Apart from this the focus of further development lies in making larger area devices and in increasing the charge collection performance in the epitaxial layer. For the former, first results in reticle stitching, that is electrically connecting IC area over the reticle border, have been encouraging (Fig. 6.12a) [356]. Full CMOS stitching over the reticle border still has to be demonstrated. The poor charge collection by thermal diffusion is another area calling for ideas. Approaches using more than one n-well collecting diode [354], a photo-FET [344,352,353], or a photo-GATE [361] have been investigated. The photo-FET technique (Fig. 6.12b) has features similar to those of DEPFET pixels (see Sect. 6.3.5). A PMOS FET is implanted in the charge collecting n-well and signal charges affect its gate voltage, thus modulating the transistor current.

Above all, the advantages of a fully CMOS monolithic device relate to the adoption of standard VLSI technology and its resulting low-cost potential (potentially $\approx$€25/cm$^2$). In turn the disadvantages also come largely from the dependence on commercial standards. The thickness of the epitaxial layer varies for different technologies. It becomes thinner for smaller processes and with it also the number of produced signal electrons vanishes. Only a few processing technologies are suited. With the rapid change of commercial process technologies this is an issue of concern. Furthermore, only NMOS devices located in a p-well can be used in the active area. PMOS transistors would require an n-well which is reserved for charge collection. The voltage signals are very small ($\approx$mV), of the same order as transis-
tor threshold dispersions requiring very low noise VLSI design. Especially in high-energy physics experiments sophisticated electronics logic, e.g. for hit readout and zero suppression, including fast clock signals must be directly implemented at the chip level. Preventing cross coupling to the tiny analog signals is a challenge. The radiation tolerance of CMOS pixel detectors for particle detection beyond \( \approx 10^{12} \text{ n}_{\text{eq}} \) is still a problem although the achieved tolerance should be sufficient for a linear collider experiment.

### 6.3.3 Monolithic SOI Pixels

In order to use high-resistivity bulk material for charge collection while maintaining CMOS processing of electronics circuits, the silicon-on-insulator (SOI) technology has been employed [362]. Figure 6.13 shows a cross-sectional view of an SOI monolithic pixel cell. By means of a thick buried oxide layer (BOX) in the bulk the active sensor volume is isolated from the electronics layers in which complete CMOS processing is now possible. At present, conventional bulk MOS technology on thick SOI substrate is still being used for prototype development [362]. Contact through the bulk oxide to the detector substrate is made by vias to p\(^+\)-implants. The detector is a conventional p\(^+\)-in-n, DC-coupled silicon detector.

The principal advantage of this pixel detector type is the possible use of very thin, high resistivity detector substrates with full charge collection in 200–300 \( \mu \text{m} \). Also, in comparison to the CMOS active pixel sensors of Sect. 6.3.2, the SOI technique offers a less restricted use of full CMOS circuitry atop the active sensor area of the device. At present the technology

![Fig. 6.13. Cross section through a SOI monolithic pixel cell. The buried oxide layer (BOX) is the insulation that separates the CMOS and sensor diode parts of the device](image)
is not a commercial standard, but would certainly become very attractive if industrial processing of bonded sensor- and CMOS-wafers became available. Commercial SOI processes have been commercially offered in the past for special radiation hard processes (e.g. the DMILL process), however without bonded high ohmic sensor substrates.

**6.3.4 Amorphous Silicon above CMOS Pixel Electronics**

Hydrogenated amorphous-silicon (a-Si:H), where the H content is up to 20%, can be put as a film on top of CMOS ASIC electronics. a-Si:H was studied as a sensor material long ago and has gained interest again [19,363], also for particle detectors, with the advancement in low-noise, low-power electronics. Early developments of a-Si:H as detector material [364,365] concluded that the signal for a minimum ionizing particle was too small to be detected. The charge signal in a film deposit of 10–30 μm thickness is 200–1,000 e− which—due to the amorphous structure—is however spread only very little and remains confined in a sensitive, almost cubic pixel volume of less than 30 μm³. The carrier mobility is very low ($\mu_e = 2–5 \text{ cm}^2/(\text{V s})$, $\mu_h = 0.005 \text{ cm}^2/(\text{V s})$). Due to the large difference in the mobilities essentially only electrons contribute to the signal. The band gap of a-Si:H is increased to 1.8 eV with respect to crystalline silicon (1.1 eV). The challenge apart from developing a-Si:H material with sufficient charge collection lies in the development of low noise (ENC < 5 e−) CMOS electronics with very low power consumption per pixel. Figure 6.14 shows a cross section of a photodiode structure realized

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**Fig. 6.14.** Cross-sectional view of a structure using a-Si:H as a sensor deposited as a film atop a CMOS circuitry. The connection to the IC is made through vias [363]
with amorphous silicon atop a CMOS circuitry [19]. From a puristic view it is more a hybrid technology, but its main disadvantage, the interconnection process, is absent. Basically any CMOS circuit and IC technology can be used and the dependence on industrial trends in IC technology is much reduced. The radiation hardness of a-Si:H detectors appears to be very high, in excess of $10^{15} \, \text{cm}^{-2}$ due to the defect tolerance, defect reversing ability of the amorphous structure, and the larger band gap. For high-Z applications polycrystalline HgI$_2$ constitutes a possible semiconductor film material. The potential advantages are small thickness, radiation hardness, and low cost. The development is still in its beginnings and for CMOS active pixel sensors—a real challenge to analog VLSI design.

### 6.3.5 DEPFET Pixels

The depleted field effect transistor (DEPFET) structure provides detection and amplification properties in every pixel jointly. The concept was proposed in 1987 [325]. It has been experimentally confirmed and successfully operated as single pixel structures [366] and as $(64 \times 64)$ pixel matrices [17, 327, 367–369].

The DEPFET detector and amplification structure is shown in Fig. 6.15. A field effect junction (JFET) or MOSFET is integrated onto a sideward-depleted detector substrate. Sideward depletion [370, 371] provides a parabolic potential with a minimum for majority carriers (electrons in the case of n-type silicon) inside the detector volume, which can be moved by appropriate biasing toward the top surface closely ($\approx 1 \, \mu\text{m}$) underneath the transistor structure. The transistor channel current can be steered by the voltage at the external gate and—important for the detector operation—also by the bulk potential. By means of a locally varying doping concentration (deep n-implant) and appropriate electrode potentials a local minimum for the charge carriers can be generated right underneath the transistor channel inside the substrate (internal gate). While (for n-type substrate material) holes created in the sensor are collected at the rear electrode, electrons are collected in the internal gate, thereby modulating the transistor current. The collected electrons are removed from the internal gate by a clear pulse applied to a dedicated CLEAR contact outside the transistor region or by other clear mechanisms, e.g. from the external gate by punch-through to the internal gate. The very low input capacitance ($\approx f\text{F}$) and the in situ amplification (i.e. charge to current conversion) of the device make DEPFET pixel detectors attractive for low-noise operation [326, 369, 372]. External amplification enters only at the second level stage. The device is controlled from two terminals, the external and the internal gate. A voltage applied to the external gate as well as collected charges $Q_{\text{sig}}$ in the potential minimum of the internal gate modulate the transistor current. The effect of the collected electrons in the internal gate on the output drain current is expressed in terms of $g_{\text{int}}^Q = \partial I_D/\partial Q_{\text{sig}}$ which is related to the transistor transconductance $g_{\text{m}}$ by
6.3 Monolithic and Semimonolithic Pixel Detectors

Fig. 6.15. The DEPFET detector and amplification structure (c) based on a sideward-depleted detector substrate material (a) with a planar field effect transistor (here MOS) embedded (b) in the pixel (from [4]). The potential shape is schematically drawn assuming ground potentials on the p⁺-implants on top and bottom surfaces and negative voltage on the n⁺ bulk contact.

The noise performance of DEPFET structures measured at room temperature is shown in Fig. 6.16 by the response to a $^{55}$Fe 6-keV X-ray source. The measured energy resolution is 134 eV for 6-keV X-rays from an $^{55}$Fe source. The low-energy tail is due to charge lost from the readout pixel by diffusion. The noise contribution is dominated by Fano noise ($\approx 14$ e⁻ at 6 keV and room temperature). The DEPFET structure itself contributes with ENC = 4.8 ± 0.1 e⁻ channel noise (insert of Fig. 6.16). With specially designed round single pixel structures, noise figures of 2.2 e⁻ have been achieved.
Figure 6.16. Response of a DEPFET pixel structure to 6-keV X-rays from an $^{55}$Fe source. The noise contribution (insert) to the signal peak is ENC = 4.8 ± 0.1 e$^{-}$.

Figure 6.17a shows the principle of operation of a complete DEPFET pixel matrix. Figure 6.17b is a photograph of the device with sequencing chips for gate control and clear, and the amplifying and scanning chip. The matrix is addressed row-wise by a gate-on voltage at the external gate and the DEPFET drain currents are read out column-wise and postamplified in the chip at the bottom.

The very good noise capabilities of DEPFET pixels are very important for low-energy X-ray astronomy and for autoradiography applications. For particle physics, where the signal charge is large in comparison, this feature can be used to design very thin detectors (≈50 µm) with very low power consumption when operated as a row-wise-selected matrix [326,374,375]. Depending on the application, i.e. aiming at very low noise operation in spectroscopy or at a very fast readout in particle physics, the device can be operated in source follower readout mode or drain current readout mode, respectively [376]. What detectors for high-energy particles is concerned, the low noise feature can be exploited to make very thin sensors, still yielding a very good S/N performance. Thinning of DEPFET-like sensors to a thickness of 50 µm using a technology based on deep anisotropic etching has been successfully demonstrated [377].

The imaging performance of DEPFET pixels can be judged in Fig. 6.18 using a matrix of 64 × 64 pixels with 50-µm pixel diameter. With 50 × 50 µm$^2$
6.3 Monolithic and Semimoniclithic Pixel Detectors

Fig. 6.17. Operation principle (top) and photograph (bottom) of a 64 × 128 DEPFET pixel system with pulsed clear. The DEPFET matrix sits in the center, CLEAR and gate-steering chips are on the sides, and the current amplifier chip is on the bottom.

Pixel cells spatial resolutions of

\[ \sigma_{xy} = 4.3 \pm 0.8 \, \text{µm} \quad \text{or} \quad 57 \pm 10 \, \text{LP/mm} \quad \text{for} \quad 22 - \text{keV} \gamma \]

\[ \sigma_{xy} = 6.7 \pm 0.7 \, \text{µm} \quad \text{or} \quad (37 \pm 3) \, \text{LP/mm} \quad \text{for} \quad 6 - \text{keV} \gamma \]

have been obtained in X-ray imaging [17].

DEPFET pixels are being developed for very different application areas: vertex detection in particle physics [326, 374, 375], X-ray astronomy [292, 293],
Fig. 6.18. Measurements of the imaging resolution of a DEPFET pixel matrix with 64 × 64 pixels and a cell size of 50-µm diameter. (a) Line contrast pattern images and (b) projection onto a plane vertical to the lines.

378], and biomedical autoradiography [17, 326, 369, 379, 380]. They are also considered in Compton camera developments [302].

For the development of DEPFET pixels for a linear collider, high readout speeds and small pixel sizes are required. Matrix row rates of 50 MHz and frame rates for 520 × 4000 pixels of 25 kHz with readout at two sides are targeted. Using implanted (DEP)MOS transistors with linear instead of circular dimensions, sensors with small cell sizes of 20 × 30 µm² have been fabricated. Complete clearing of the internal gate, which is important for high-speed on-chip pedestal subtraction, has been demonstrated[326]. A large matrix is read out using sequencer chips for row selection and clear, and a column readout chip based on current amplification and storage as shown in Fig. 6.17(bottom). With a power duty cycle of on/off = 1:200 the power consumption for a five-layer, 1.2-m² DEPFET pixel vertex detector is estimated to be as small as 5 W [326], rendering a very low mass detector without cooling pipes feasible. Radiation resistance of the system at a linear collider is required to several kilograys [345]. As expected for MOS devices, charge trapping in the interface (SiO₂ and Si₃N₄) leads to transistor threshold shifts which has been measured to amount to ∼2–4 V for ionizing doses up to 10 kGy [381]. Threshold shifts in this voltage range can be conveniently compensated by a corresponding adjustment of the voltage levels delivered by the sequencer chips, provided that the shifts occur fairly homogeneously over the area of a detector.